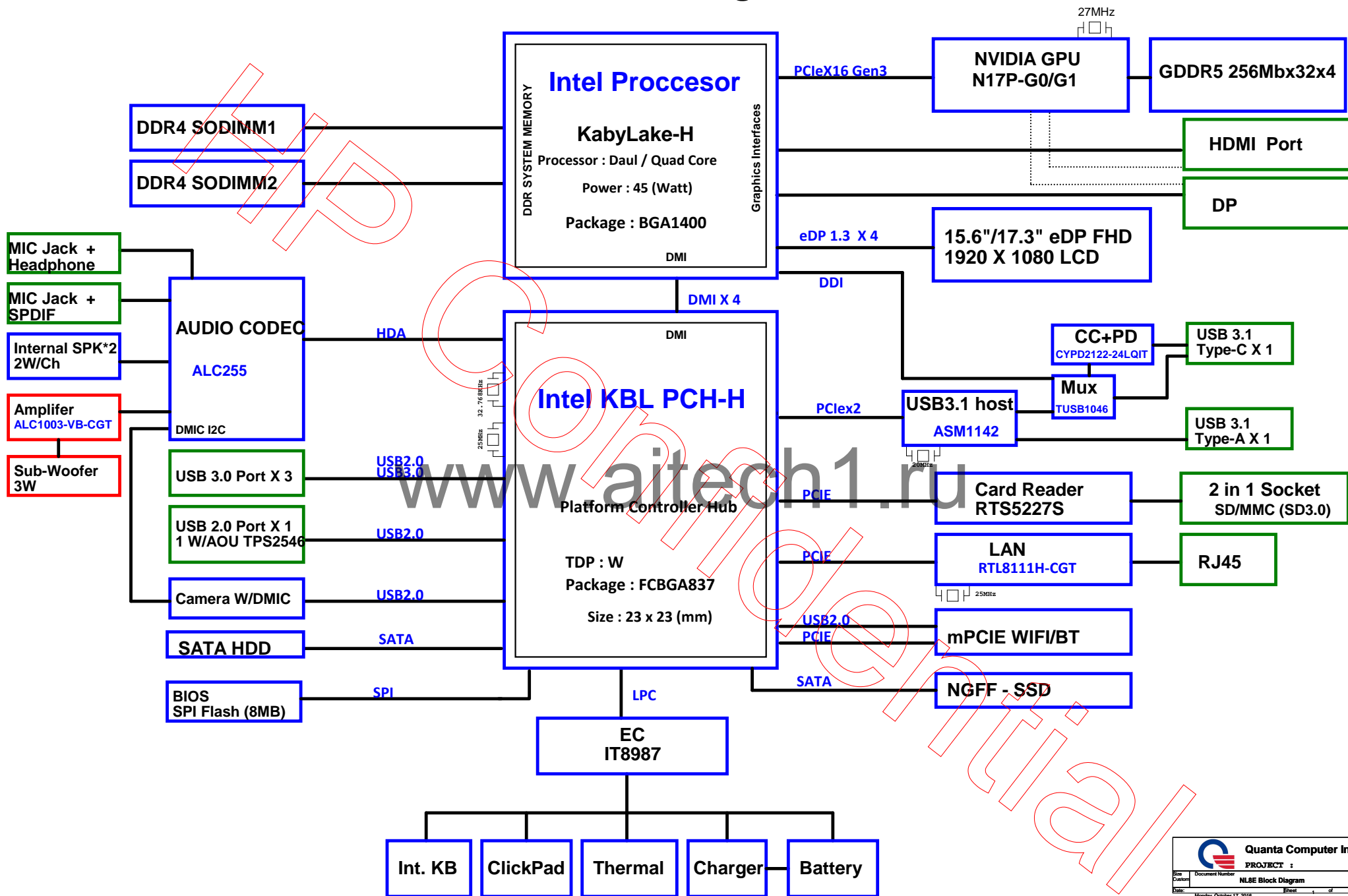
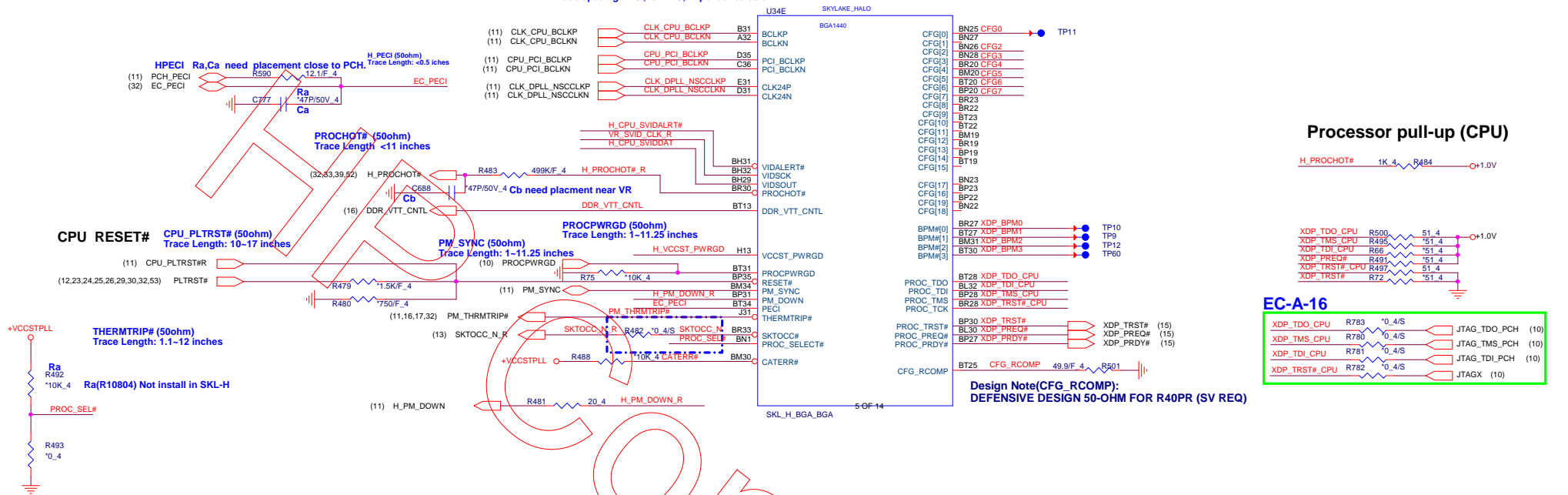


NL8K Block Diagram

01



Host CLK:
Trace length < 11000 MILS
Trace spacing = 15 ,20 MILS, Impedence 90 ohm



CPU CORE SVID

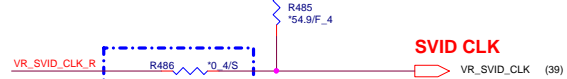
Layout note: need routing together and ALERT need between CLK and DATA.

**CLOSE TO CPU
PLACE THE PU RESISTORS**



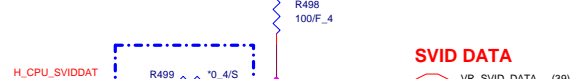
SVID ALERT

PLACE THE PU RESISTORS
CLOSE TO VR
PULL UP IS IN THE VR MODULE



SVID CLK

**CLOSE TO CPU
PLACE THE PU RESISTORS**



SVID DATA

CFG

0 Enable; SET DFX_ENABLED BIT IN DEBUG

1 , Disable;

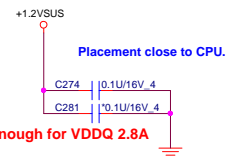
Configuration Signals:		The CFG signals have a default value of '1' if not terminated on the board.	
CFG[0]	Stall reset sequence after PCU PLL lock until de-asserted	Note that some of the Intel reference designs board might connect CFG[0] to HOOK[2]. This route is not needed on a Oxm board.	
CFG[2]	PCI Express Static Lane Reversal	x1 = Normal operation x0 = Lane numbers reversed	
CFG[4]	eDP enable	x1 = Disabled x0 = Enabled	
CFG[6.5]	PCI Express Bifurcation	x00 = 1 x8 & 2 x4 PCI Express	
		x01 = reserved x10 = 2 x8 PCI Express x11 = 1 x16 PCI Express	
CFG[7]	PEG defer training	x1 = PEG train follow RESETB de-asserted x0 = PEG wait for BIOS fro training	

HWPD

R10479 close to CPU side
H_VCCST_PWRGD trace 0.3" - 1.5"



CPU VDDQ



Note: please keep plane is enough for V



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PROJECT :

02 -- SKYPAKE 1/20

REV	1
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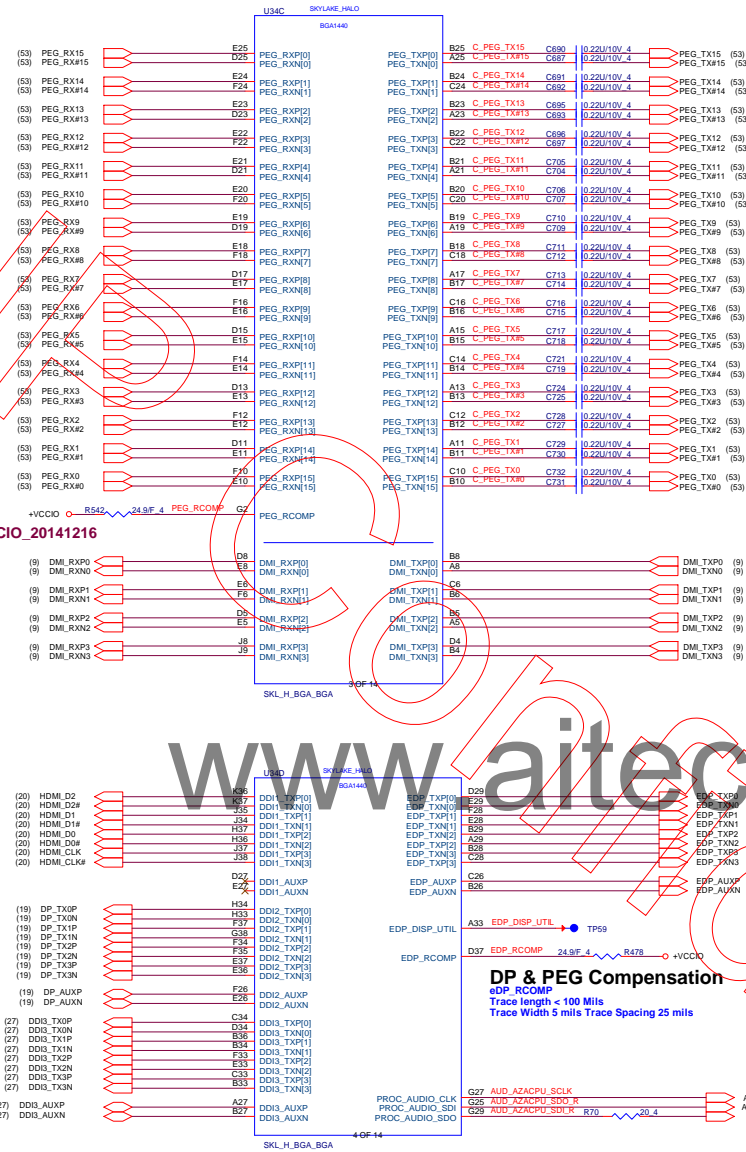
PEG_RCOMP
Trace length < 400 MILS
Trace width = 5 MILS
Trace spacing = 15 MILS

Change PWR rail from +1.0V to +VCCIO_20141216

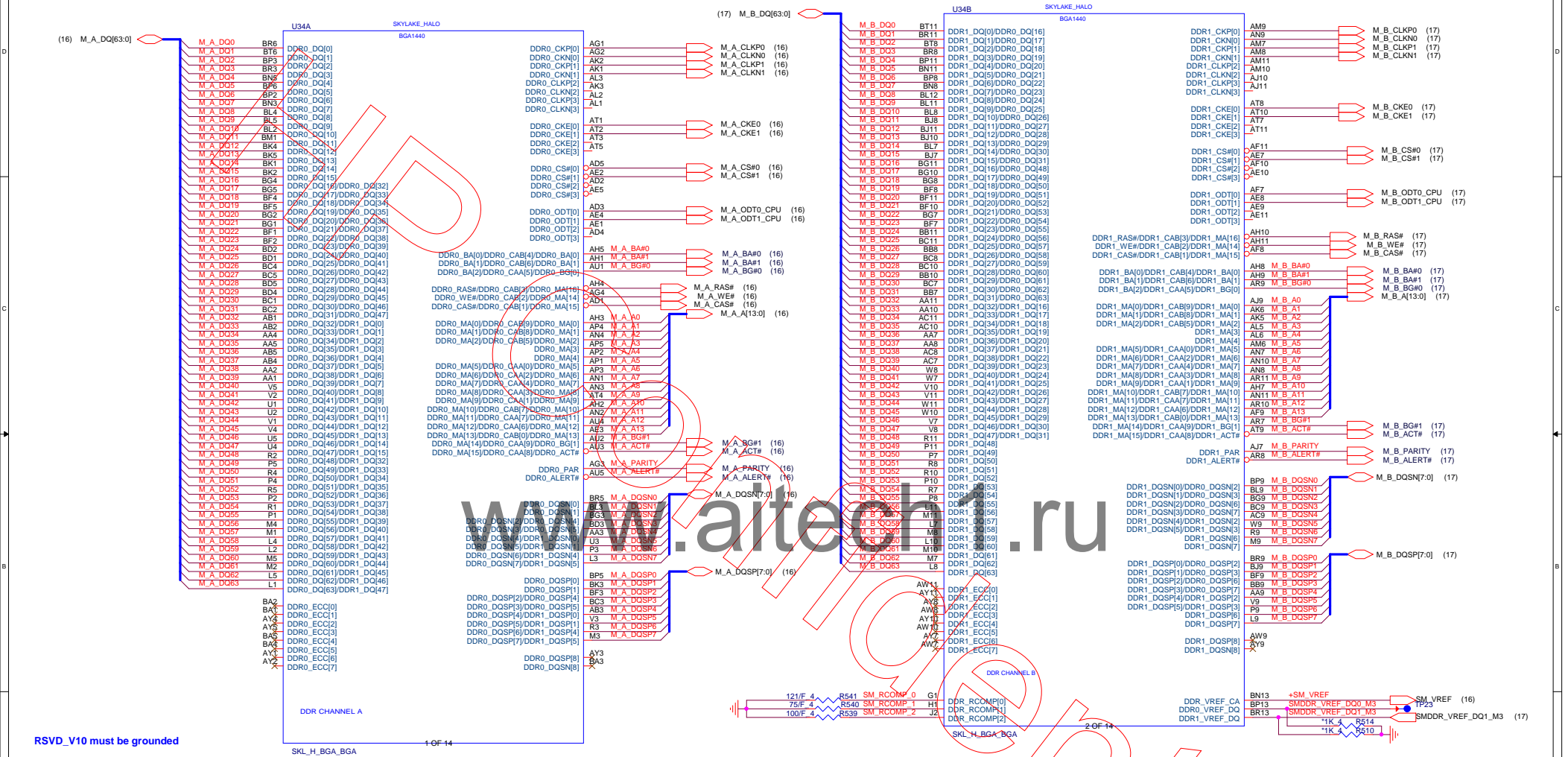
HDMI

DP

USB3.1 type-C



SKYLAKE Processor (DDR4)




Follow SKL H EDS page 133 to 45W(GT4+OPC): +VCCGT=104A/12A (GTx)
Follow SKL H EDS page 133 to 45W(GT2): +VCCGT=55A

4+4e, Support eDRAM Only, GTX 12A

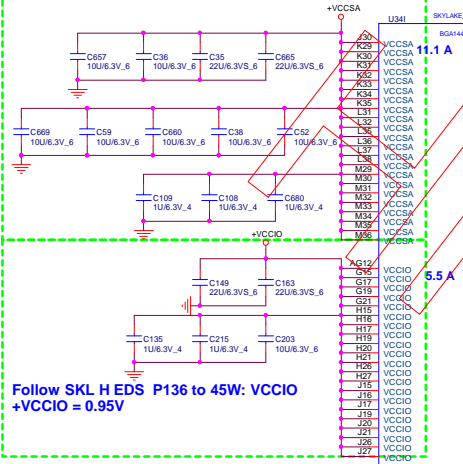
+VCC_CORE (40,44,7)
+1.2VSSUS (10,16,17,2,35,43,44,50,6)



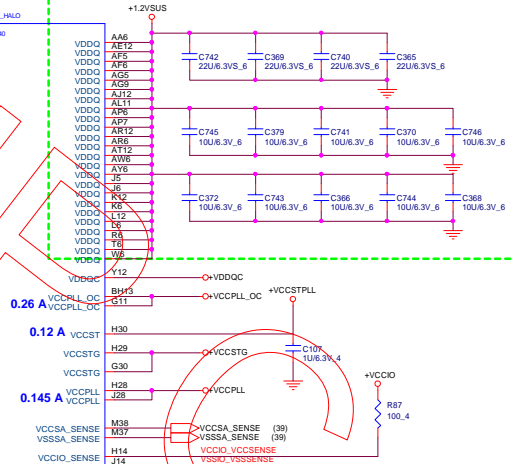
VCC Output Decoupling Recommendations		

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		66

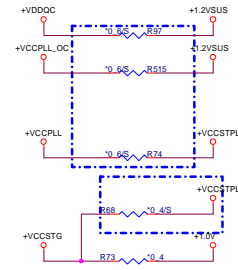
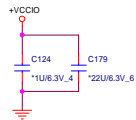
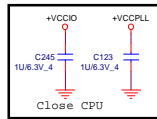
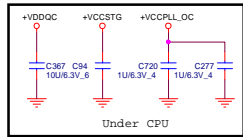
Follow SKL H EDS page 135 to 45W(GT2): VCCSA=11.1A (GTx)



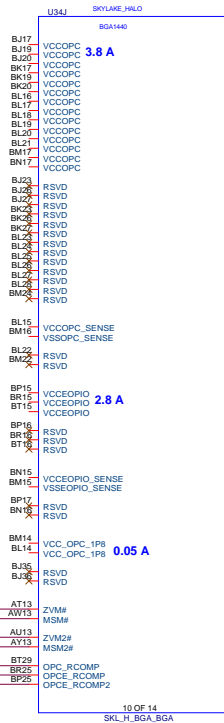
Follow SKL H EDS page 135 45W: VDDQ=2.8A



Follow SKL H EDS P136 to 45W: VCCIO
+VCCIO = 0.95V



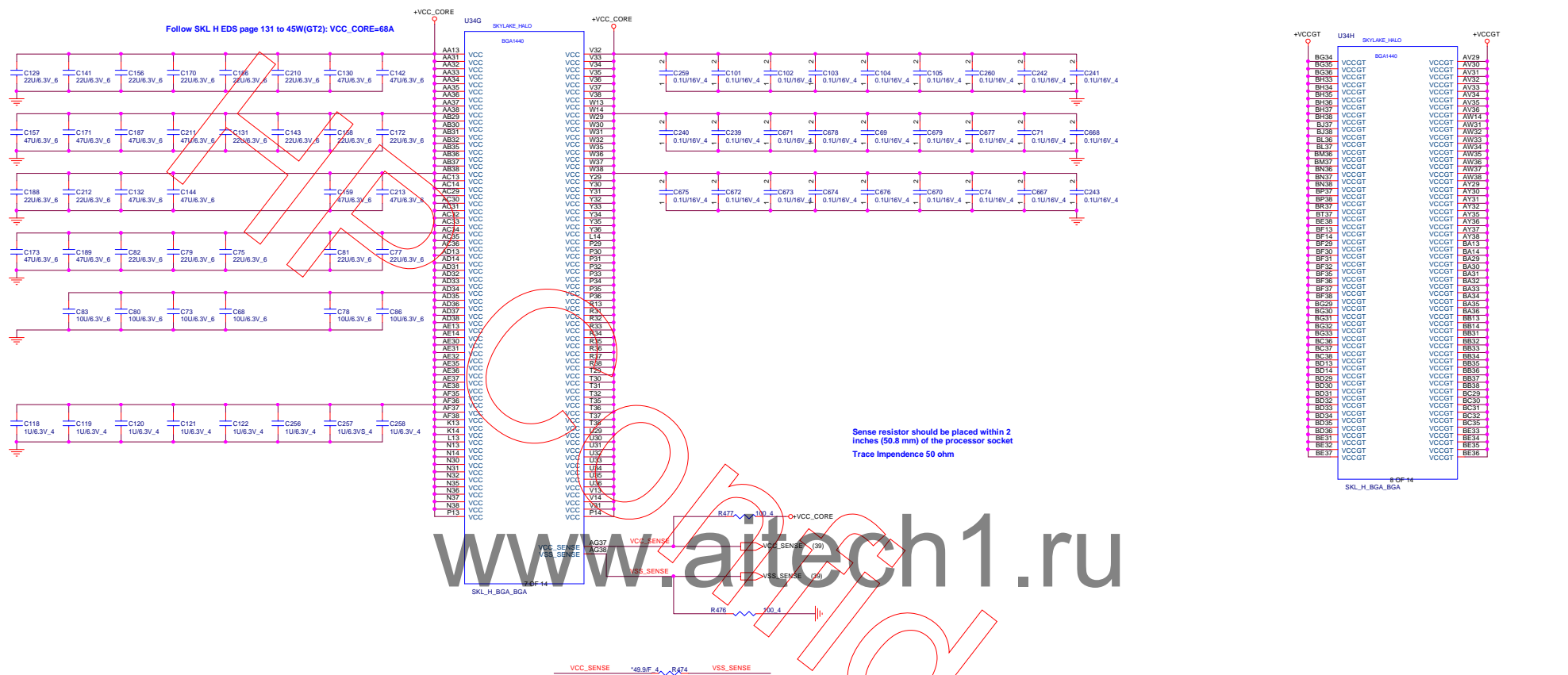
EDRAM Only, PLACE CAPS IN ACK SIDE



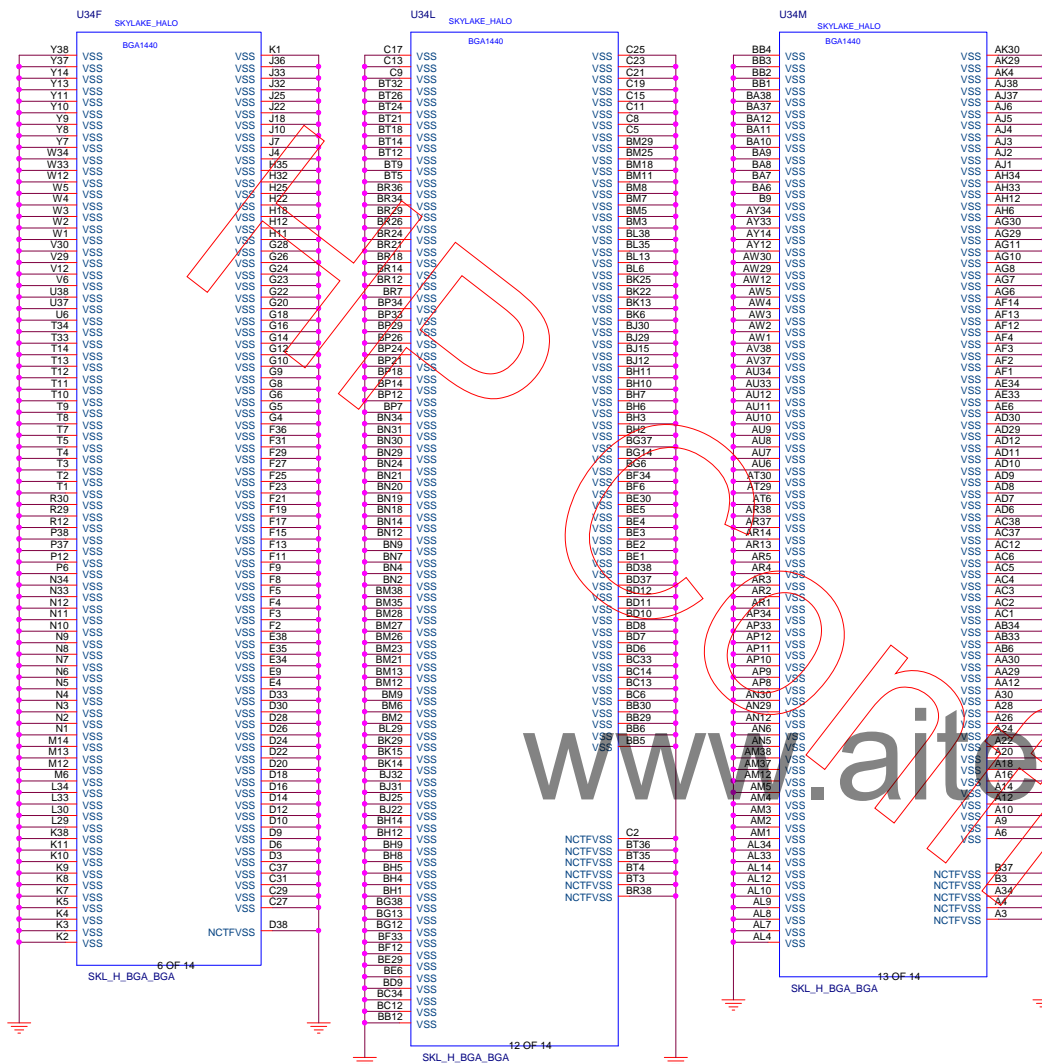
Unconnected for Processors without OPC.

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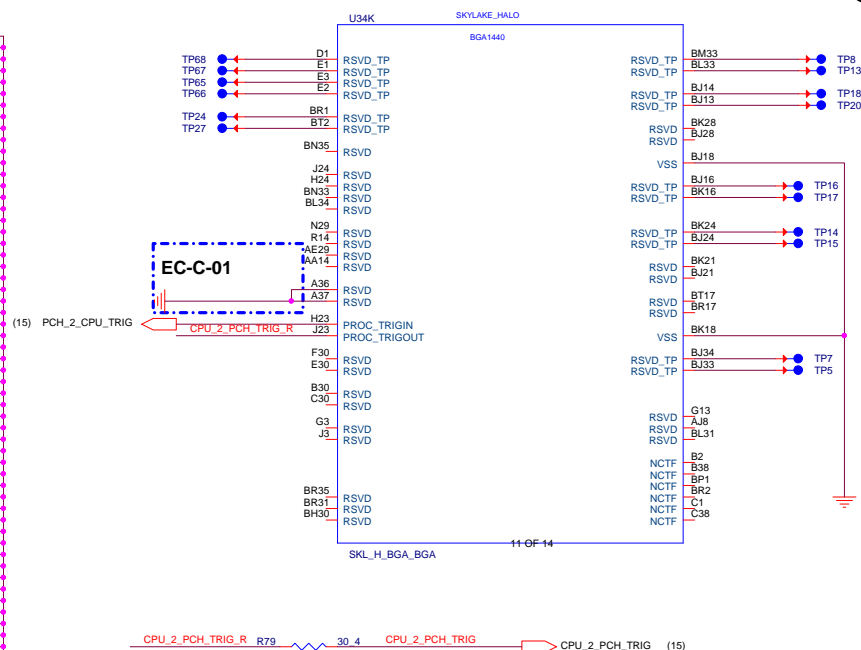
Follow SKL H EDS page 131 to 45W(GT2): VCC_CORE=68A

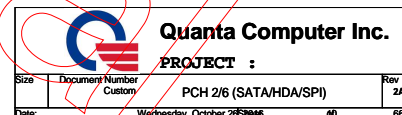
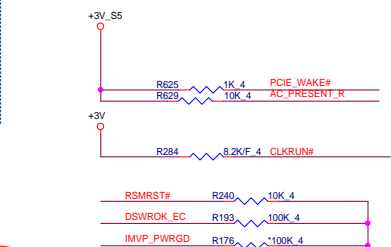


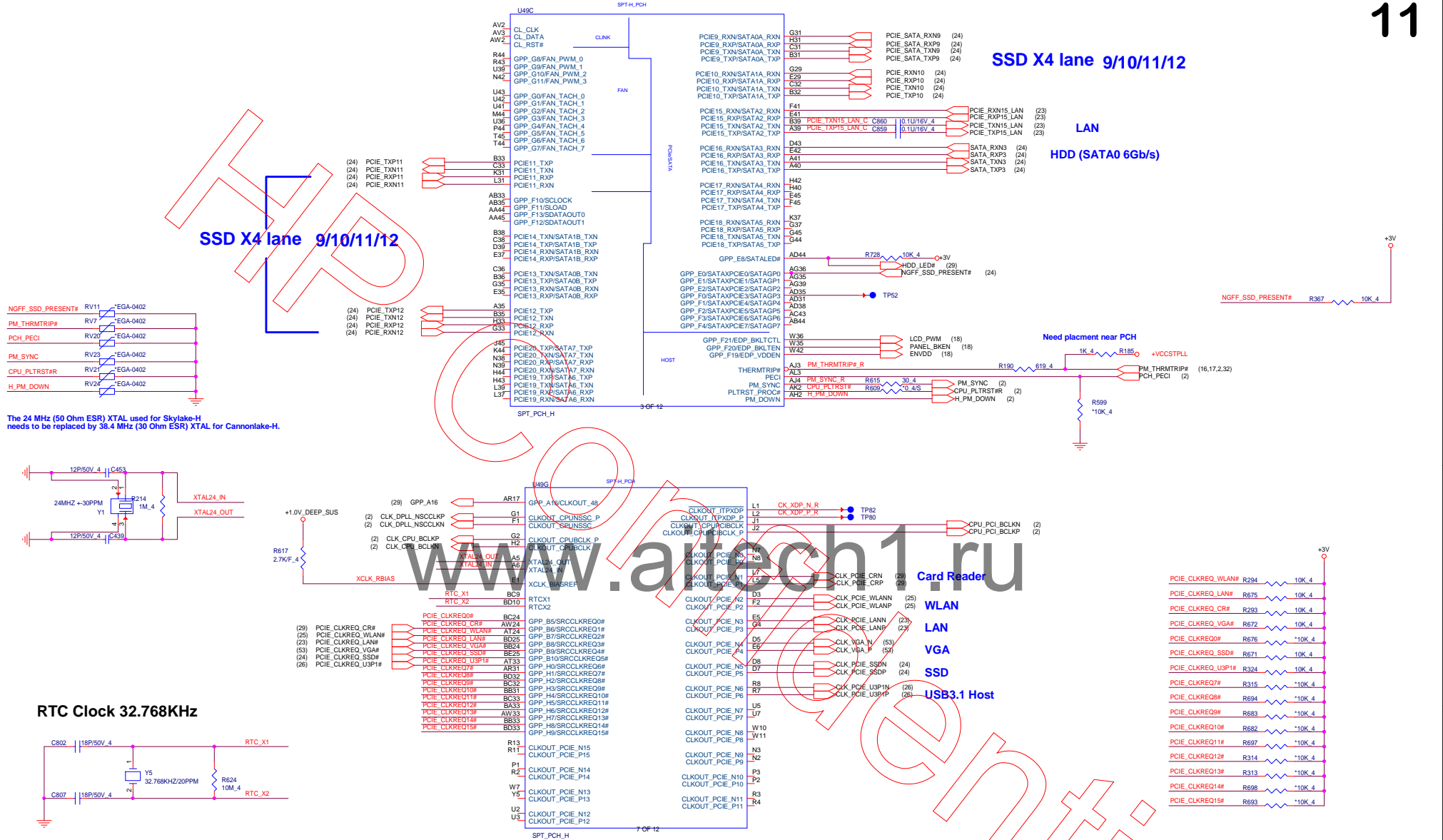
Haswell Processor (GND)

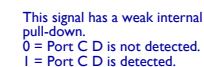
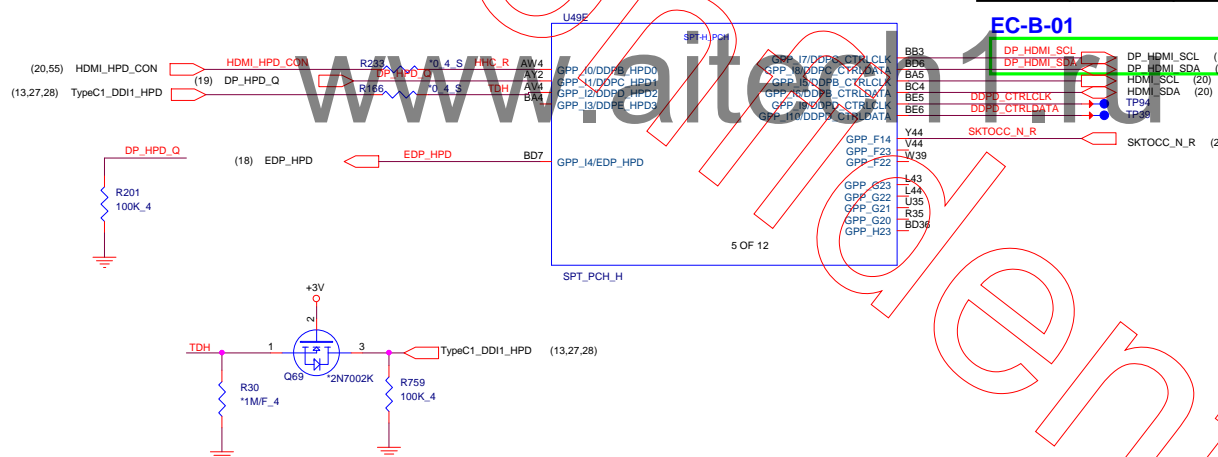
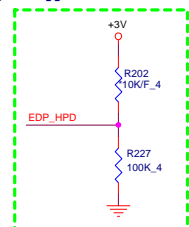
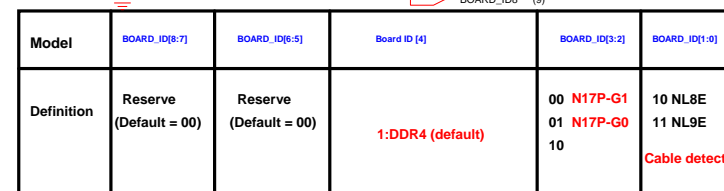


Haswell Processor (RESERVED, CFG)

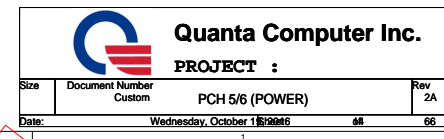


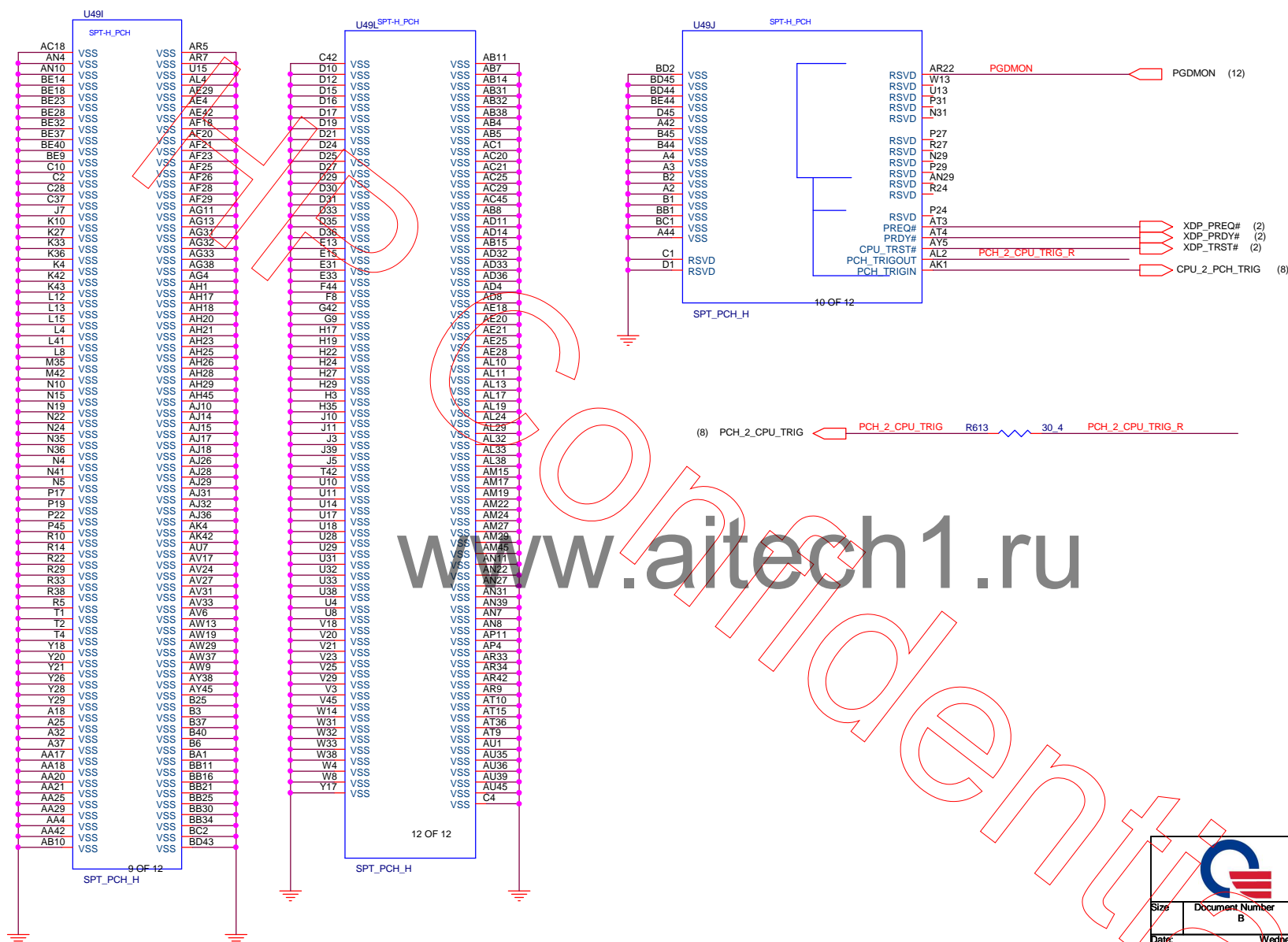


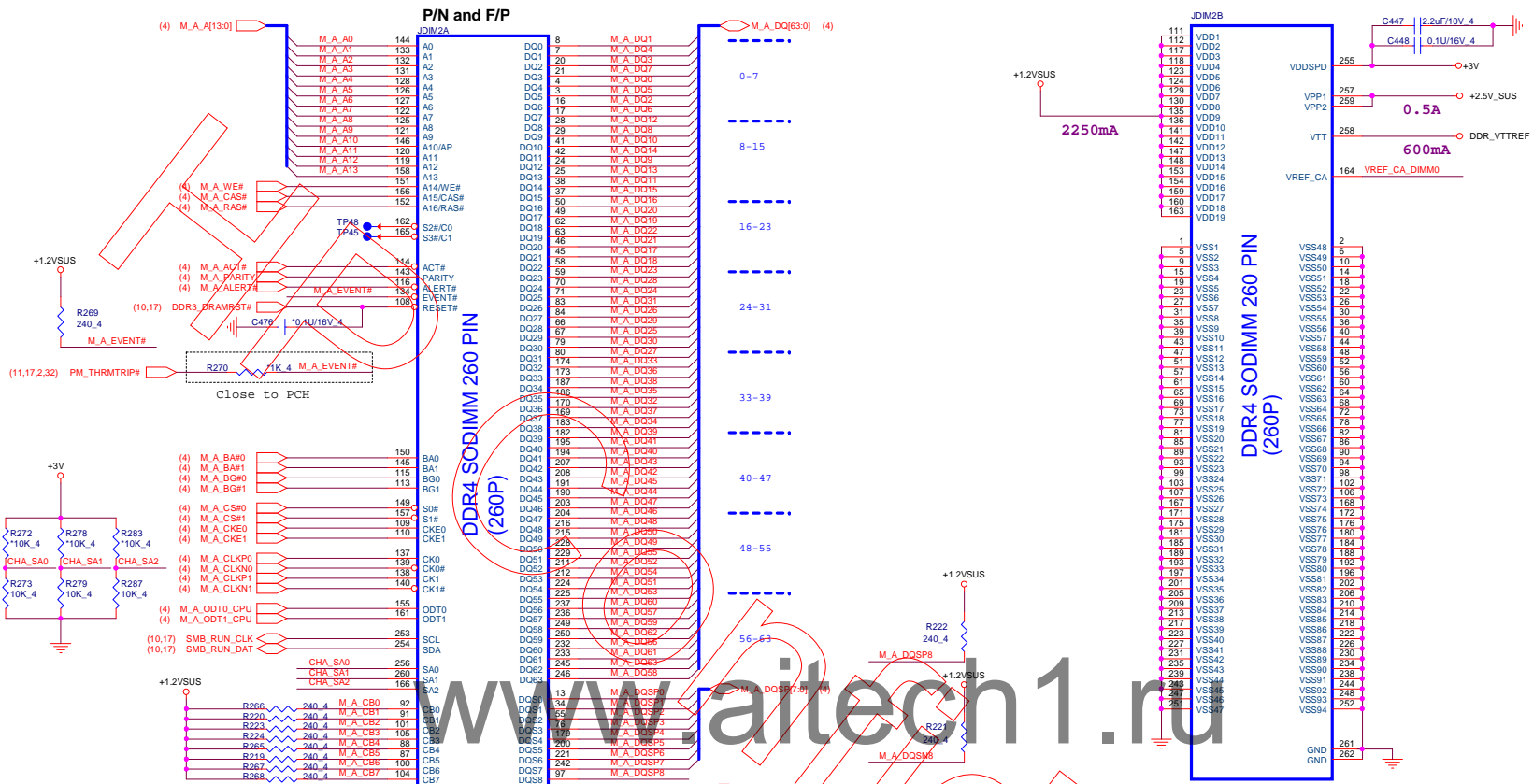


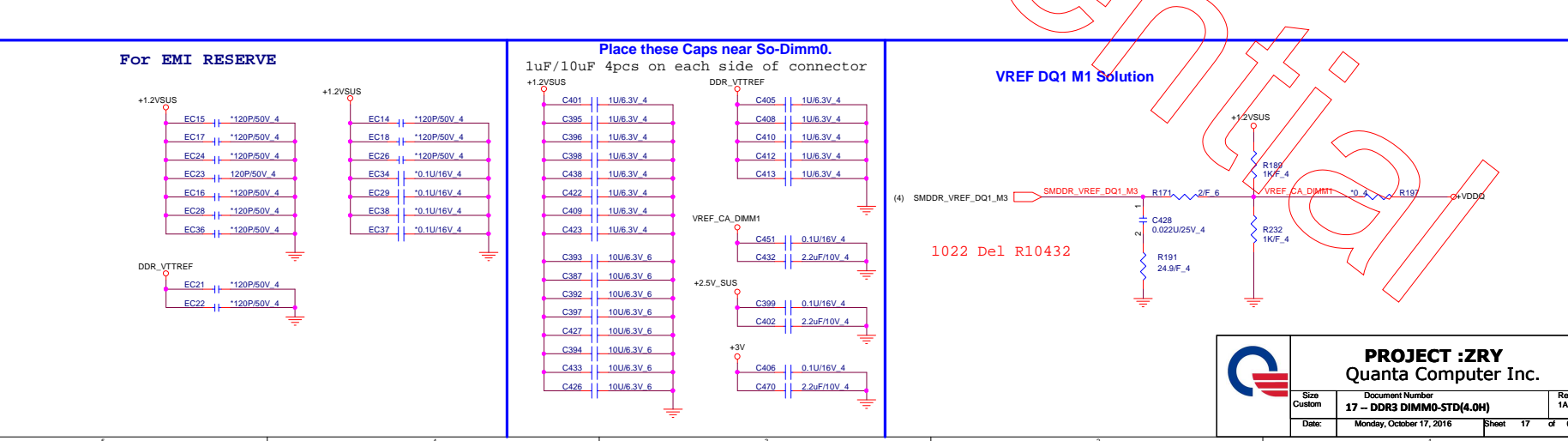


EC-B-01



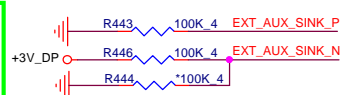
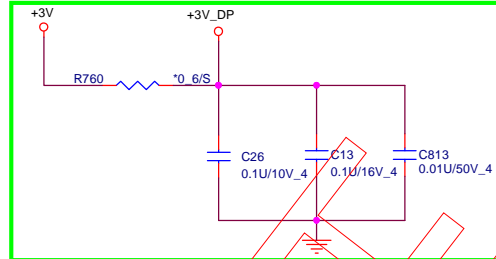






EC-A-01

EC-B-02

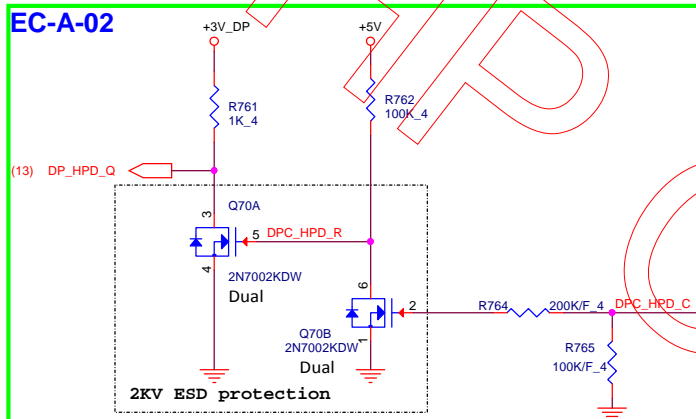


(10,11,12,13,14,16,17,18,20,21,22,23,24,26,27,28,29,30,31,32,36,43,45,50,52,9) +3V
(20,21,22,24,30,31,43,45,52,63) +5V

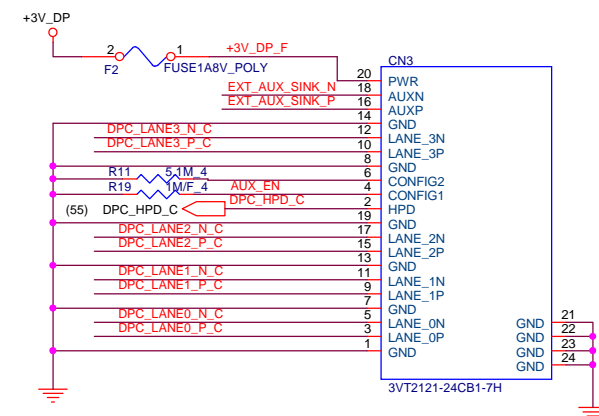
+3V
+5V

19

EC-A-02



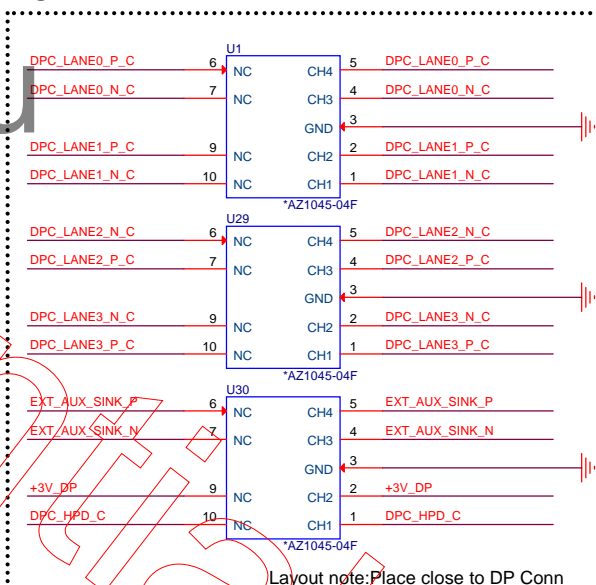
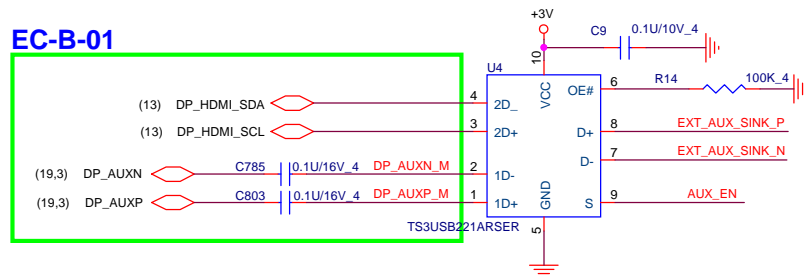
(3) DP_TX0P	C613	0.1U/16V_4	DPC_LANE0_P_C
(3) DP_TX0N	C614	0.1U/16V_4	DPC_LANE0_N_C
(3) DP_TX1P	C5	0.1U/16V_4	DPC_LANE1_P_C
(3) DP_TX1N	C6	0.1U/16V_4	DPC_LANE1_N_C
(3) DP_TX2P	C15	0.1U/16V_4	DPC_LANE2_P_C
(3) DP_TX2N	C16	0.1U/16V_4	DPC_LANE2_N_C
(3) DP_TX3P	C622	0.1U/16V_4	DPC_LANE3_P_C
(3) DP_TX3N	C623	0.1U/16V_4	DPC_LANE3_N_C



For ESD

(19,3) DP_AUXP	R457	*0.4	DP_AUXP_R	C628	0.1U/16V_4	EXT_AUX_SINK_P
(19,3) DP_AUXN	R456	*0.4	DP_AUXN_R	C627	0.1U/16V_4	EXT_AUX_SINK_N

EC-B-01



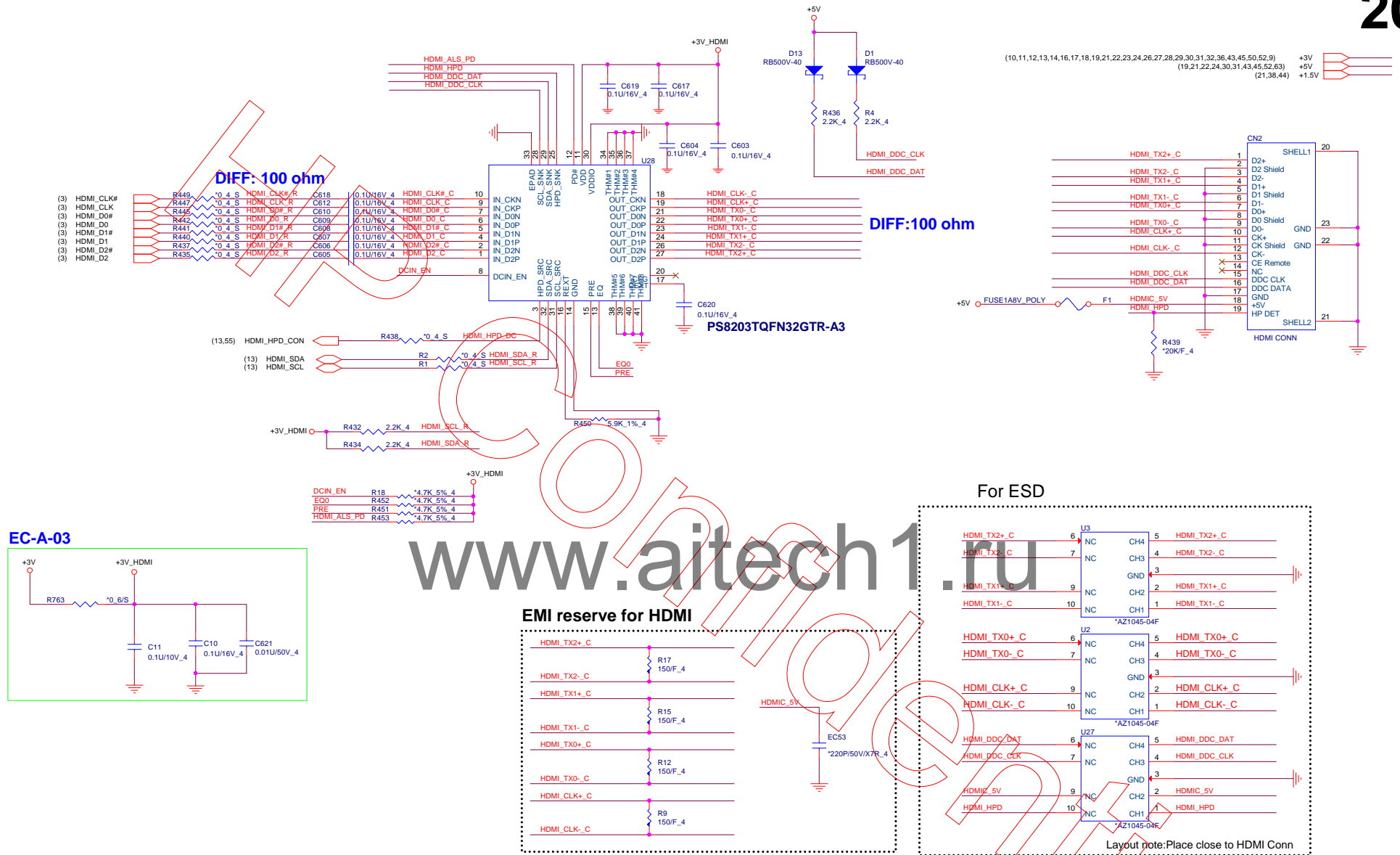
Layout note: Place close to DP Conn

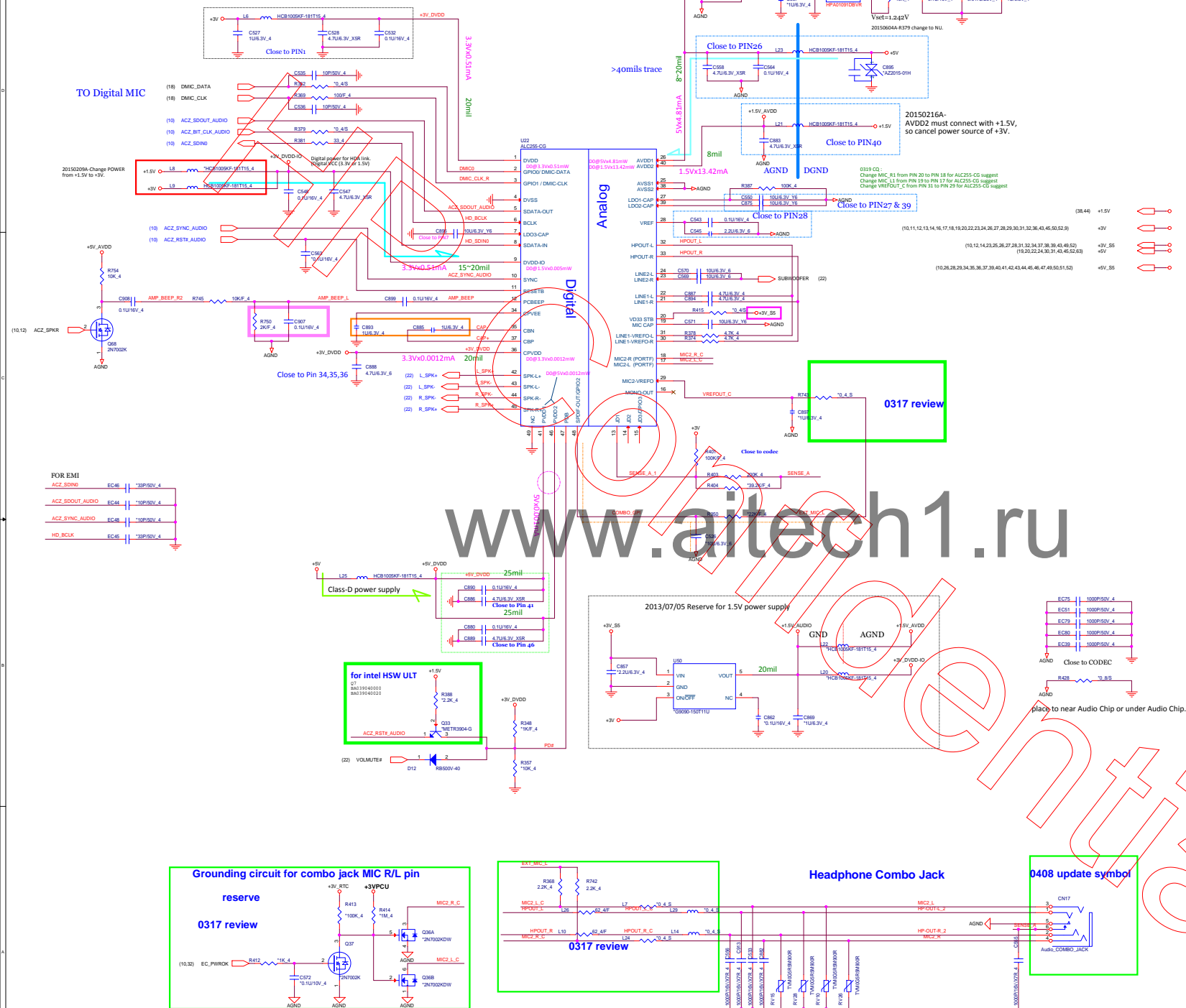


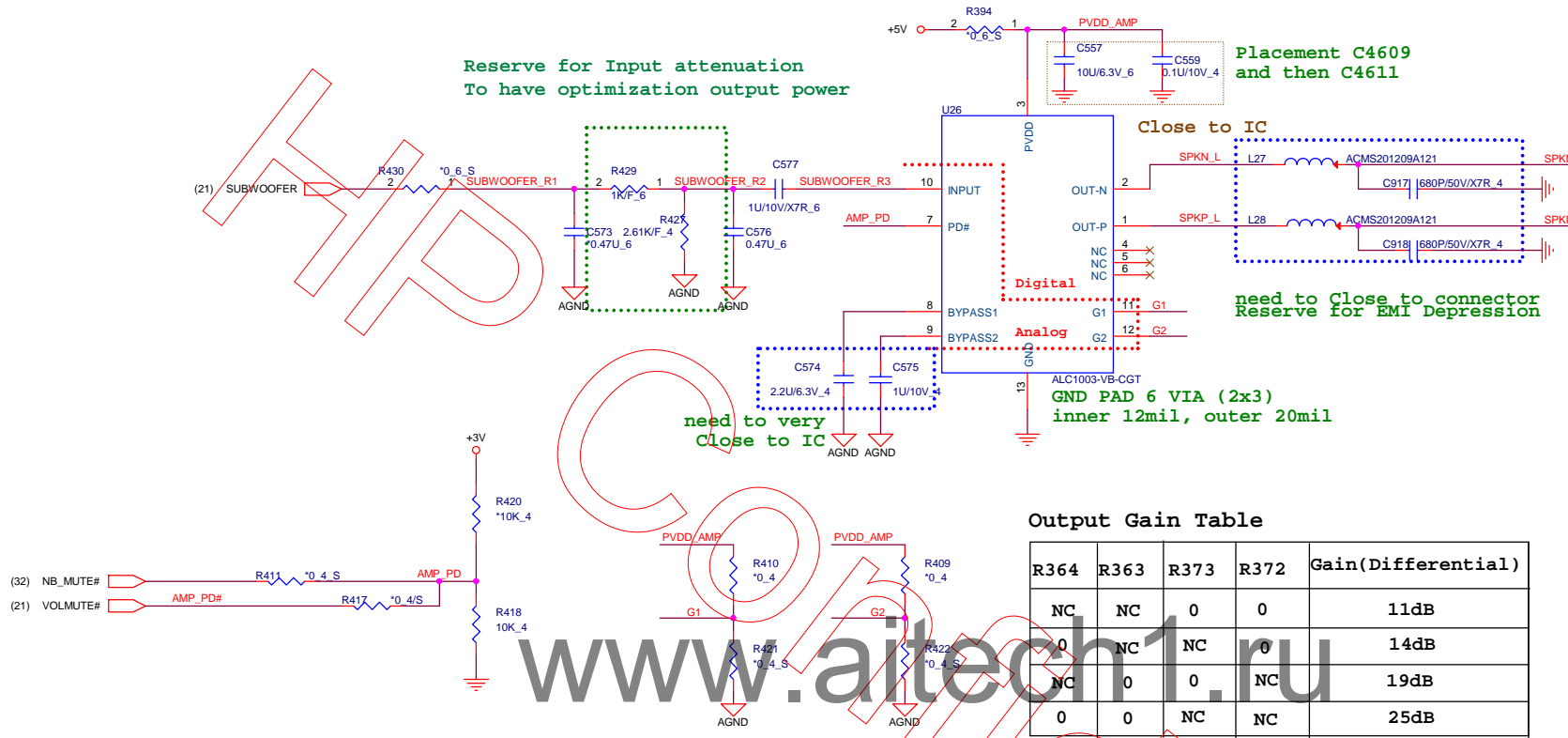
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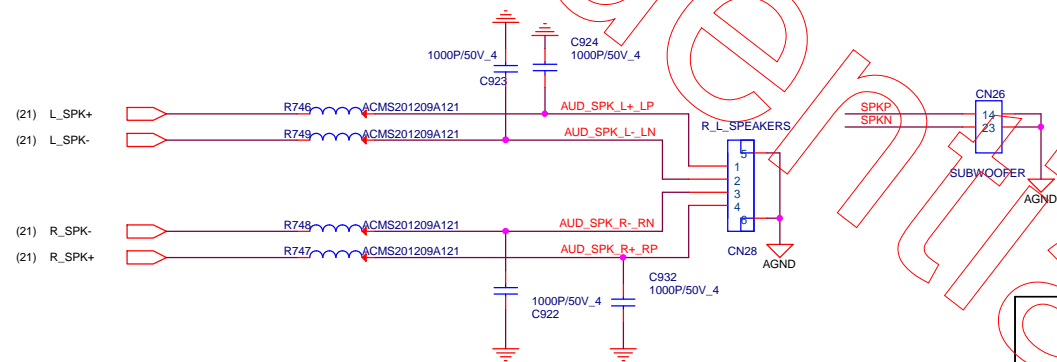


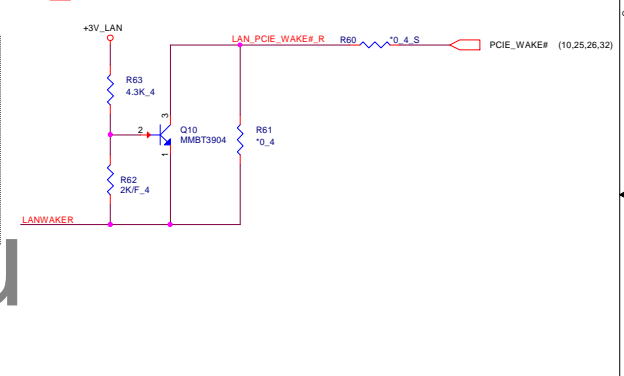
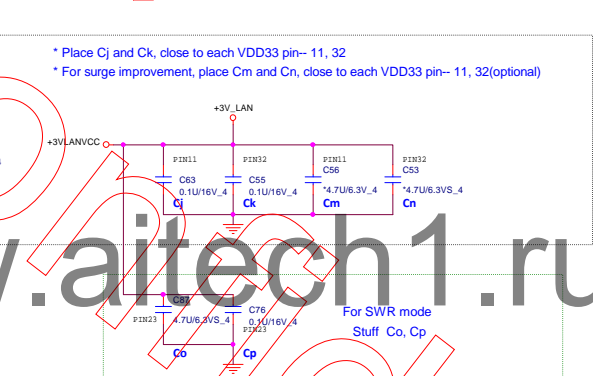
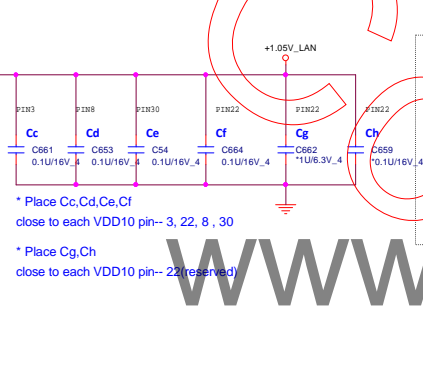
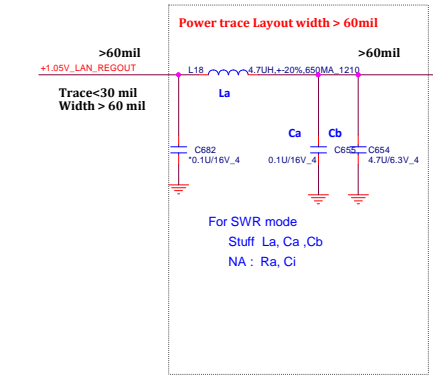
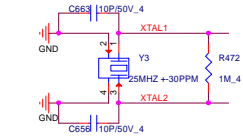
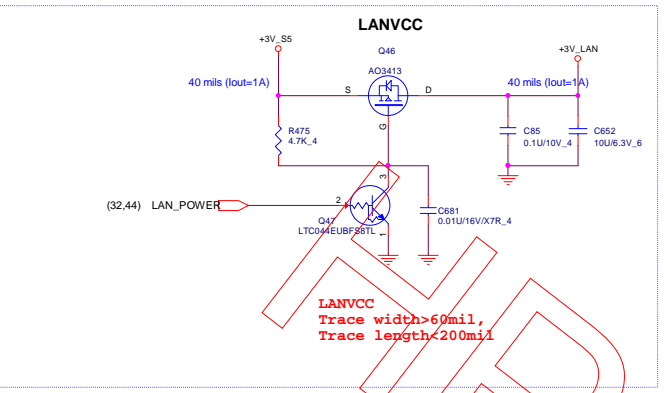


Output Gain Table

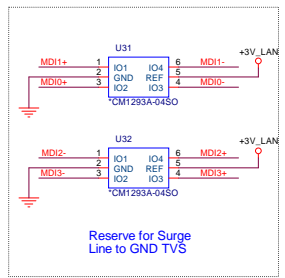
R364	R363	R373	R372	Gain(Differential)
NC	NC	0	0	11dB
0	NC	NC	0	14dB
NC	0	0	NC	19dB
0	0	NC	NC	25dB

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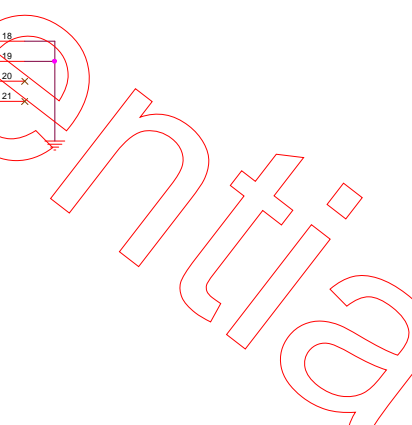
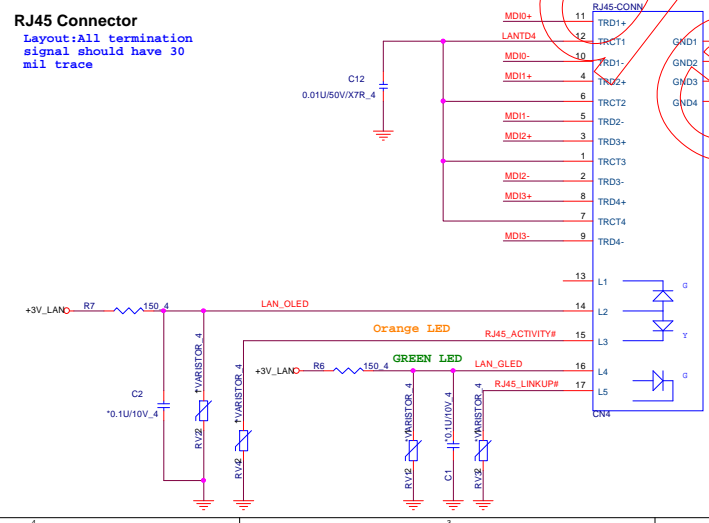


Transformer



RJ45 Connector

Layout: All termination signal should have 30 mil trace



RJ45 Connector

SSD

(10,11,12,13,14,16,17,18,19,20,21,22,23,26,27,28,29,30,31,32,36,43,45,50,52,9)

+3V

(19,20,21,22,30,31,43,45,52,63)

+5V

24

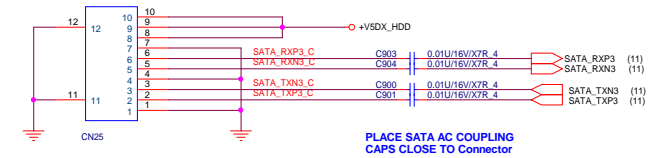
HDD

DC Current rating: 2 A (MAX)

80 mils (out=2A)



HDD_CONN



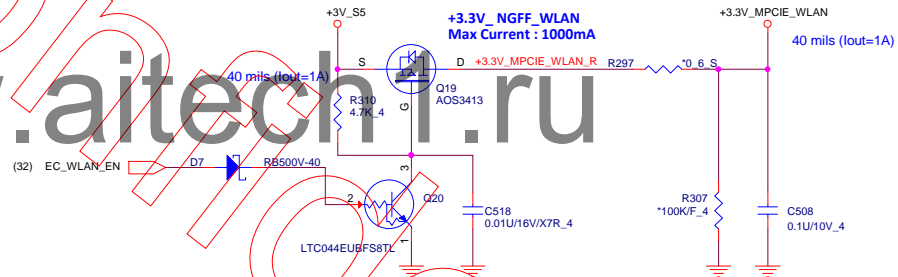
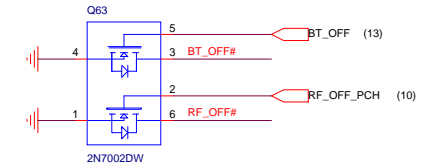
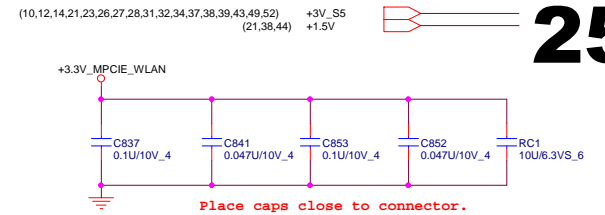
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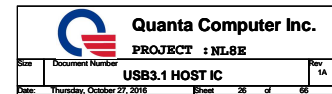
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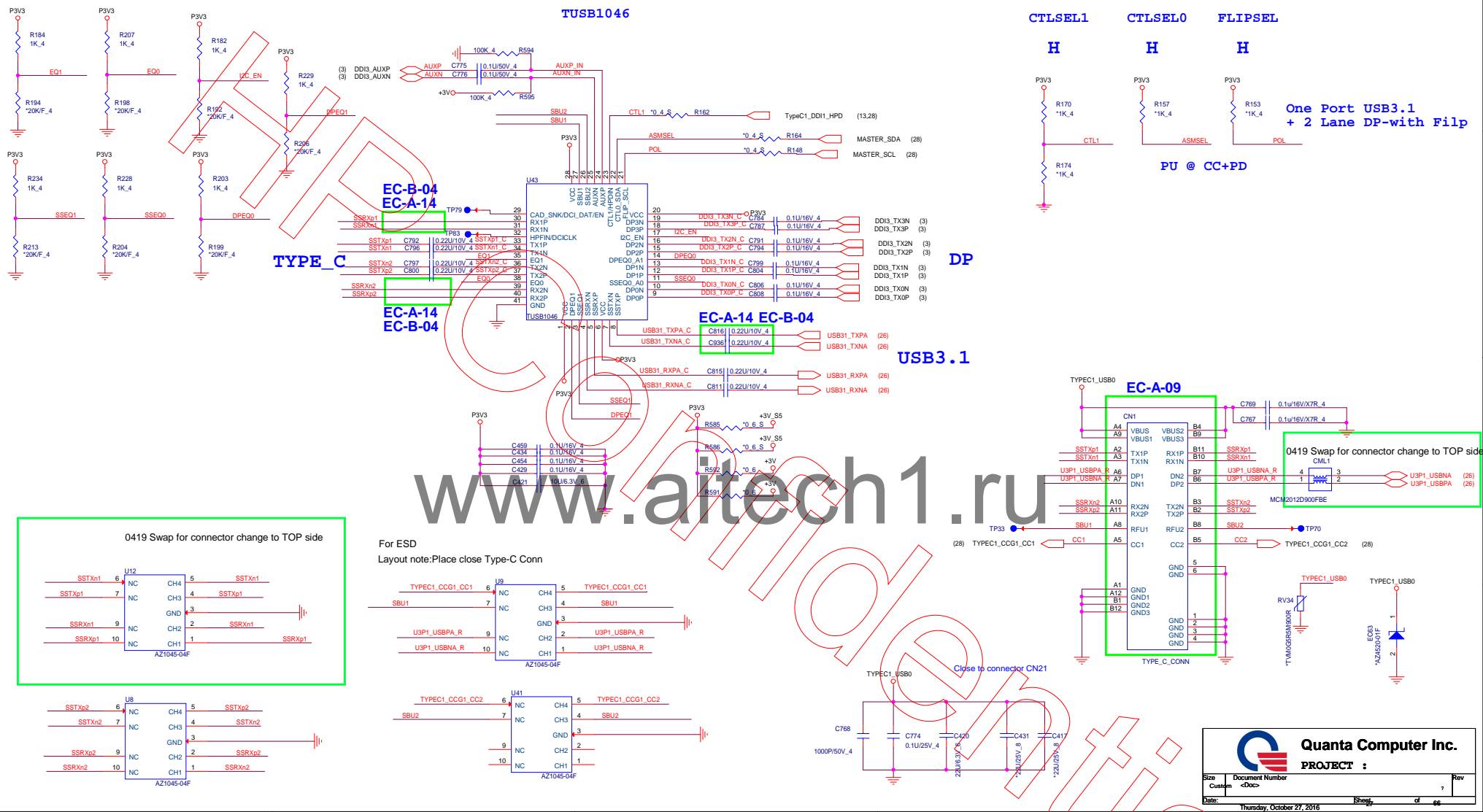
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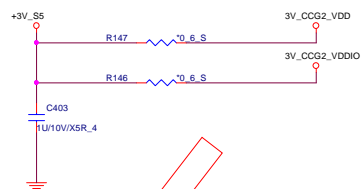
25



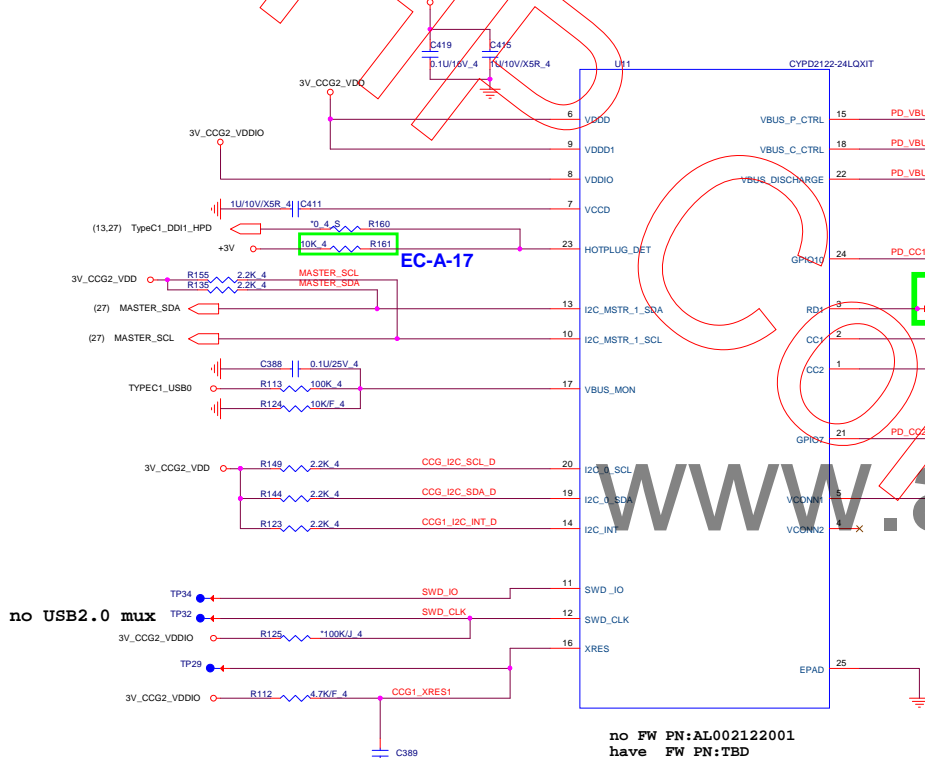




CC+PD



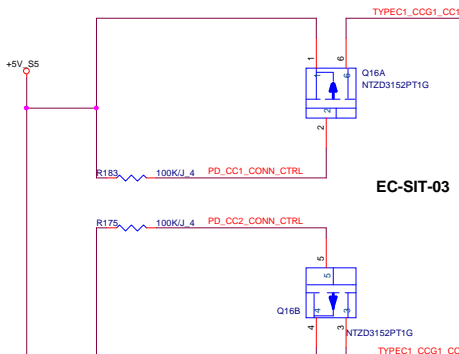
CCG2 Connections



This project is DFP only,
please floating RD pin.

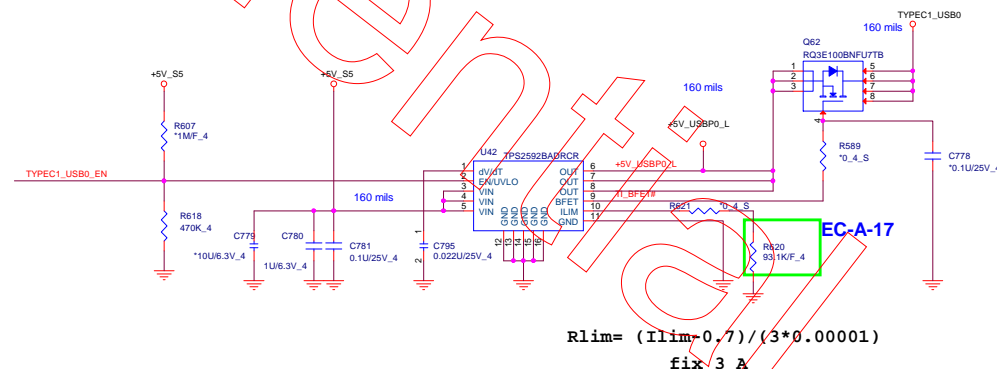
(10,26,29,34,35,36,37,39,40,41,42,43,44,45,46,47,49,50,51,52) +5V_S5
(10,12,14,21,23,25,26,27,31,32,34,37,38,39,43,49,52) +3V_S5
(27,44) TYPEC1_USB0

EC-SIT-03



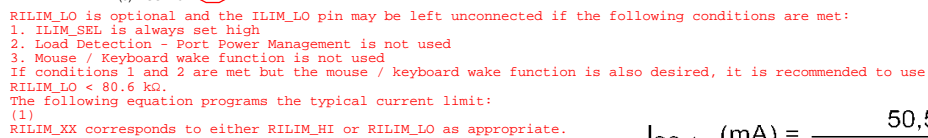
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no FW PN:AL002122001
have FW PN:TBD

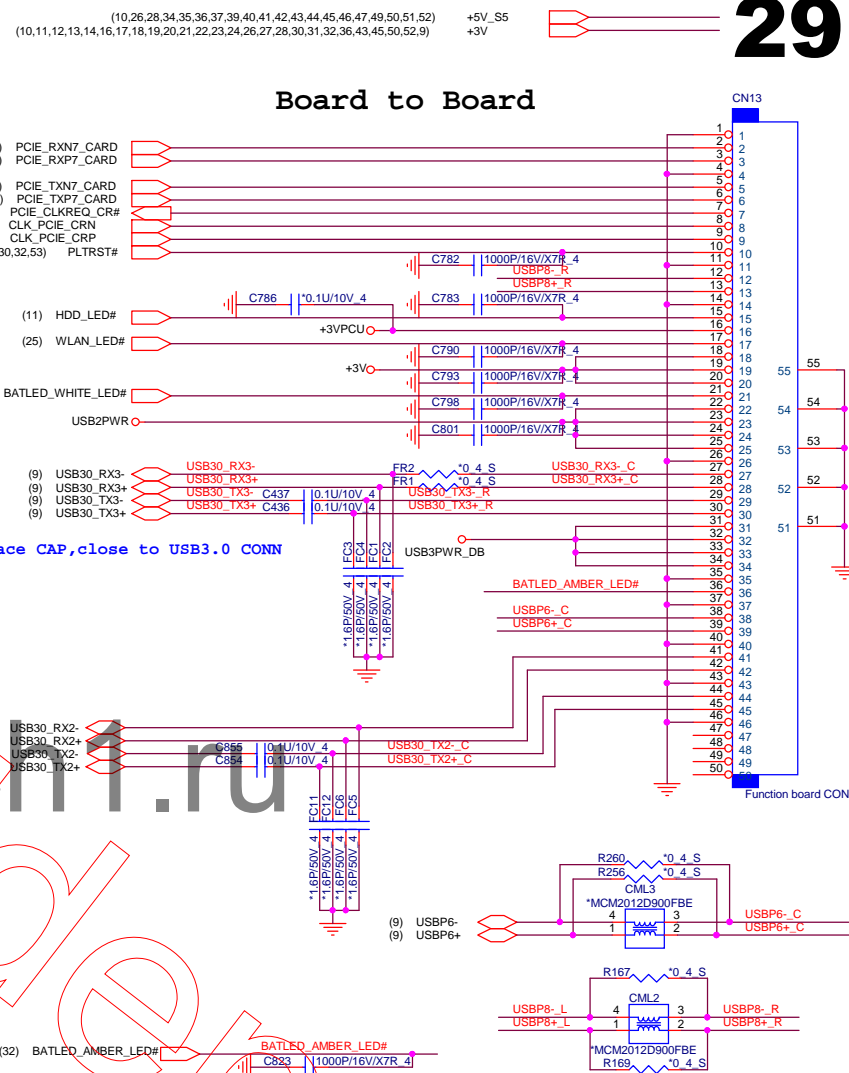


$$R_{lim} = (I_{lim} - 0.7) / (3 \times 0.00001)$$

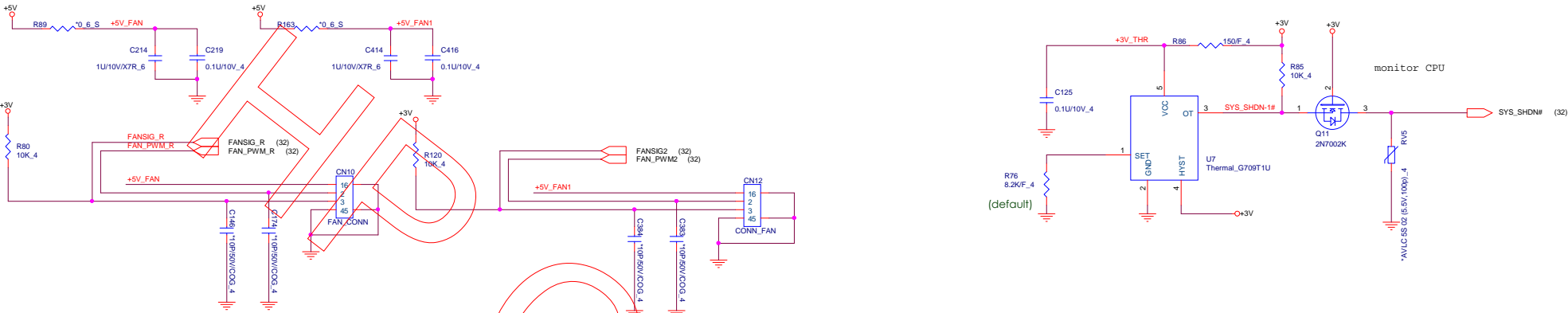
fix 3 A



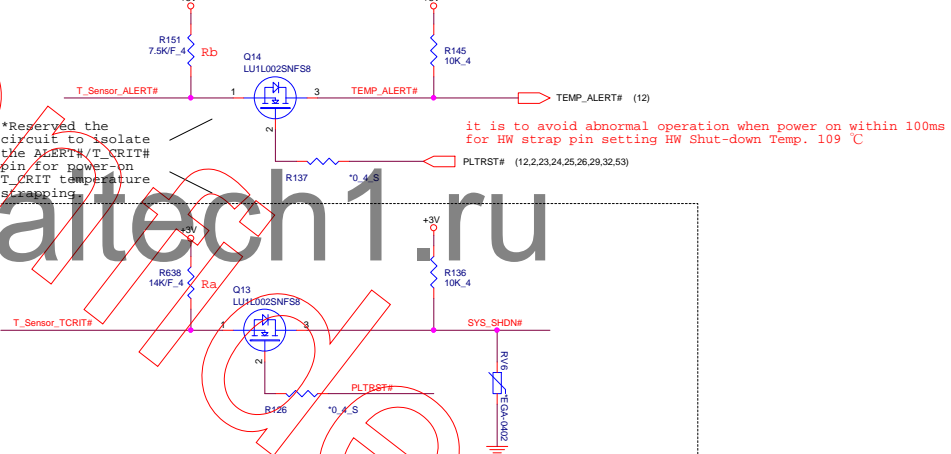
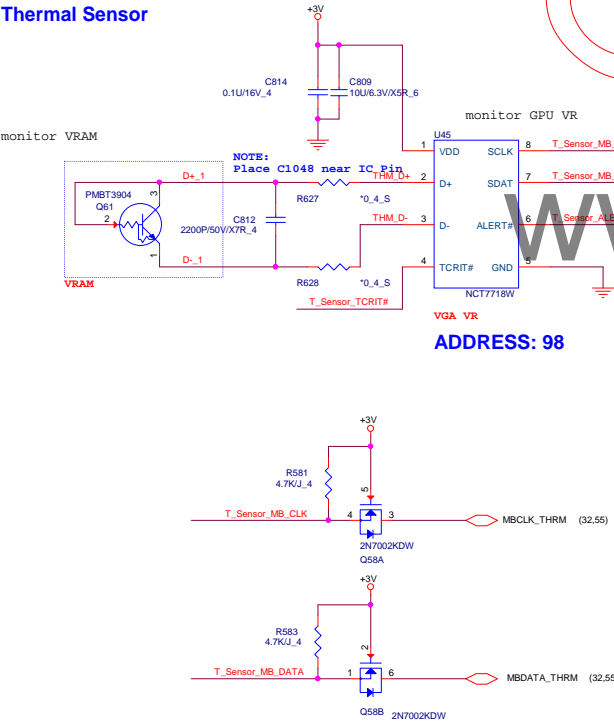
$$I_{OS_typ}(mA) = \frac{50,500}{(R_{IILIM_xx}(k\Omega) + 0.1)}$$



Thermal Sensor



Thermal Sensor



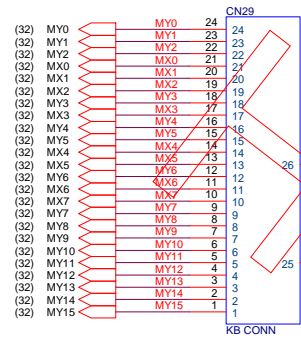
ALERT# /T_CRIT#

Pull-up Resistor

Rb	2Kohm	7.5Kohm	Ra	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77°C	87°C	97°C	107°C	117°C	
7.5Kohm	79°C	89°C	99°C	109°C	119°C	
10.5Kohm	81°C	91°C	101°C	111°C	121°C	
14Kohm	83°C	93°C	103°C	113°C	123°C	
18.7Kohm	85°C	95°C	105°C	115°C	125°C	

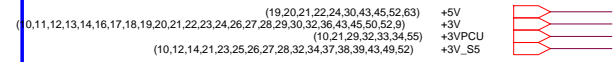
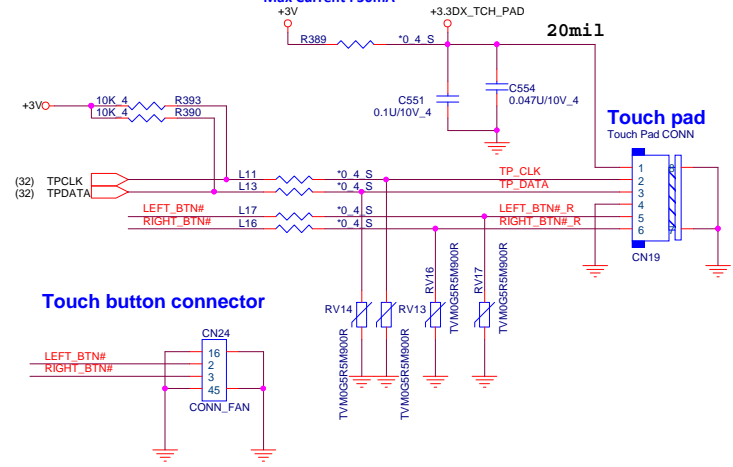
T_CRIT temperature strapping point

KEYBOARD

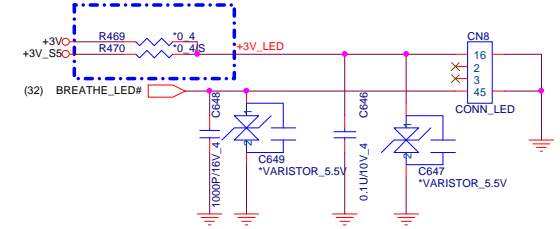
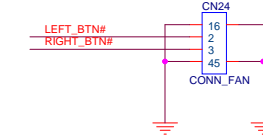


For EMI

MY15	C589	220P/50V/X7R 4	C591	220P/50V/X7R 4	MY13
MY10	C588	220P/50V/X7R 4	C590	220P/50V/X7R 4	MY12
MY11	C589	220P/50V/X7R 4	C600	220P/50V/X7R 4	MY3
MY14	C592	220P/50V/X7R 4	C582	220P/50V/X7R 4	MY6
MX0	C597	220P/50V/X7R 4	C598	220P/50V/X7R 4	MX1
MY1	C595	220P/50V/X7R 4	C584	220P/50V/X7R 4	MX7
MY5	C579	220P/50V/X7R 4	C583	220P/50V/X7R 4	MX6
MX3	C601	220P/50V/X7R 4	C587	220P/50V/X7R 4	MY9
MX2	C599	220P/50V/X7R 4	C586	220P/50V/X7R 4	MY8
MY0	C594	220P/50V/X7R 4	C585	220P/50V/X7R 4	MY7
MY5	C581	220P/50V/X7R 4	C578	220P/50V/X7R 4	MY4
MX4	C580	220P/50V/X7R 4	C596	220P/50V/X7R 4	MY2

+3V_TP
Max Current : 50mATouch pad
Touch Pad CONN

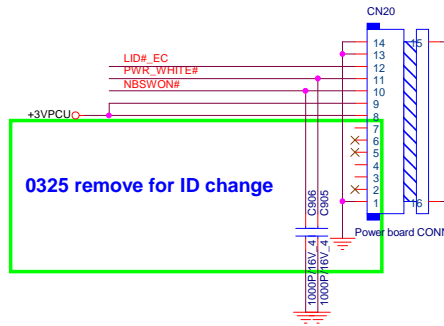
Touch button connector



CONN_LED

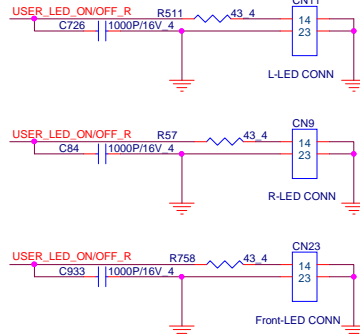
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Power board for NL8

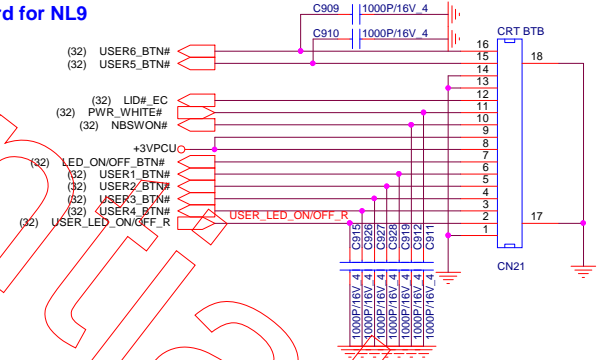


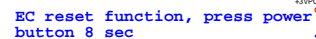
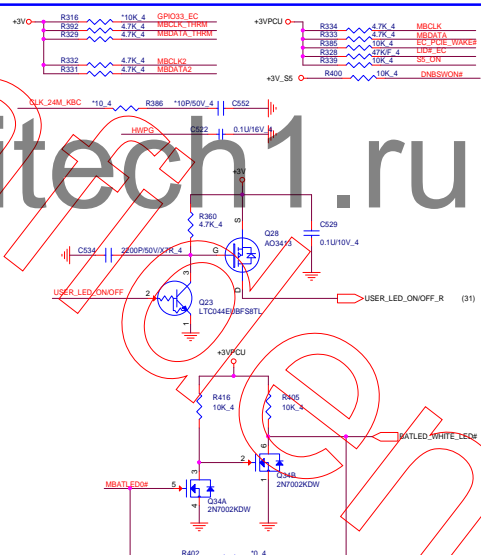
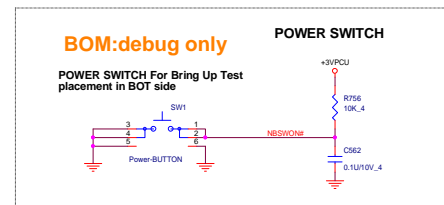
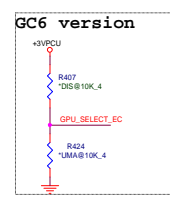
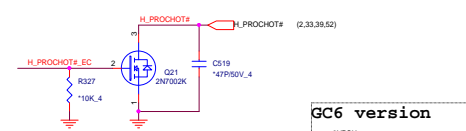
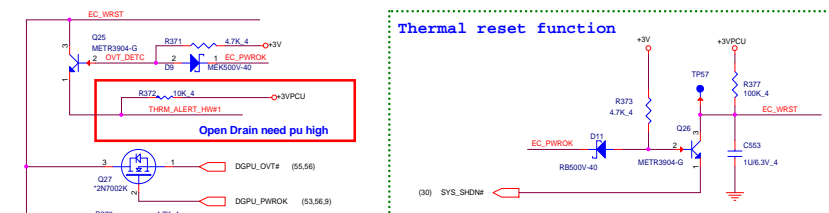
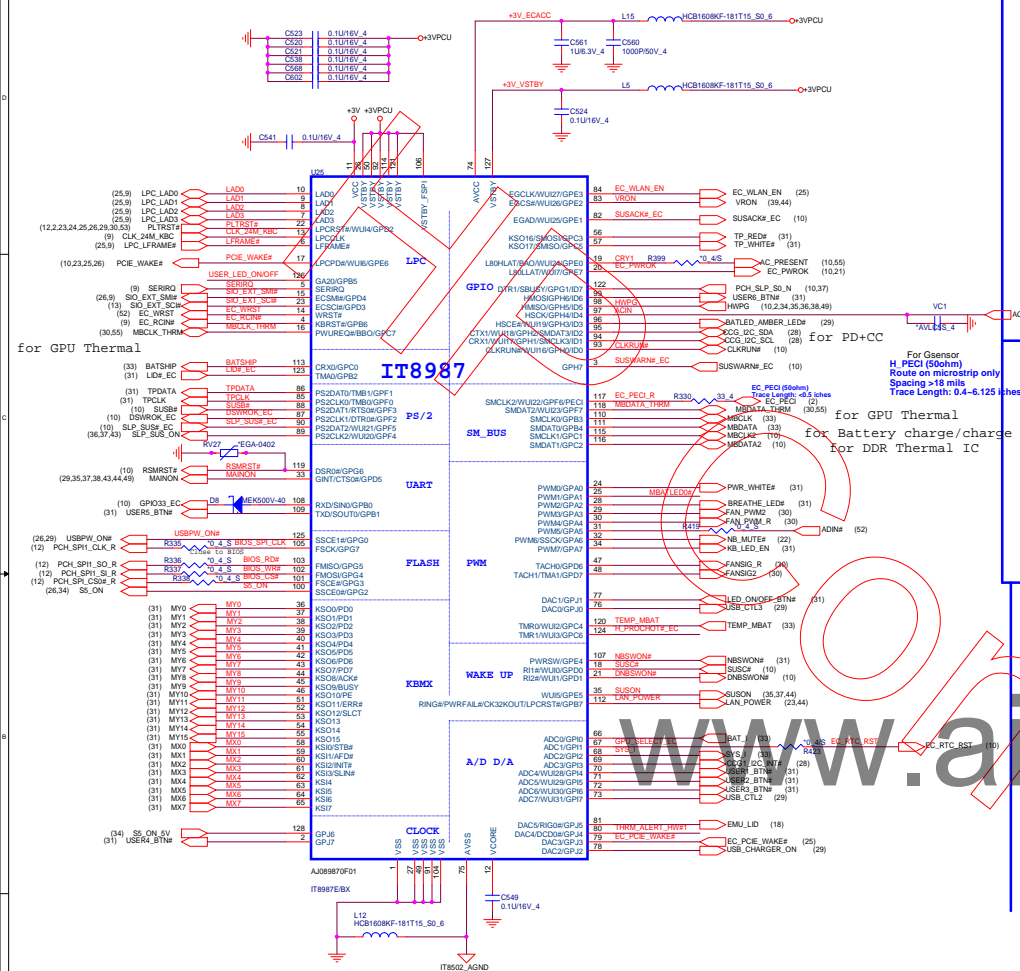
0325 remove for ID change

LED CONN



Power board for NL9





(18,34,36,38,40,41,42,47,50,52,53)
(10,21,29,31,32,34,55)



33

230W for N17E-G1 ; N17P-G1
180W for N16E-GT (970M)
150W for N16P-GX (960M) ; N16E-GS (965M)
120W for N16P-GT (950M)

System Adaptor
DC-IN

Do Not add test pad on BATDIS_G signal

Place this ZVS close to Diode away +VIN

EMI request for ISN

5m ohm for 180W adaptor

Place this ZVS close to Far-Far away +VIN

Place this cap close to EC

For ISN

Place this cap close to EC

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Place this cap close to EC

Place this cap close to EC

Place this cap close to EC

VIDCHG = 8 or 16 x (VSRN - VSRP)

Quanta Computer Inc.	
PROJECT : Charger (BQ24780S)	
Rev	Rev
Custom	36
Friday, October 28, 2016	



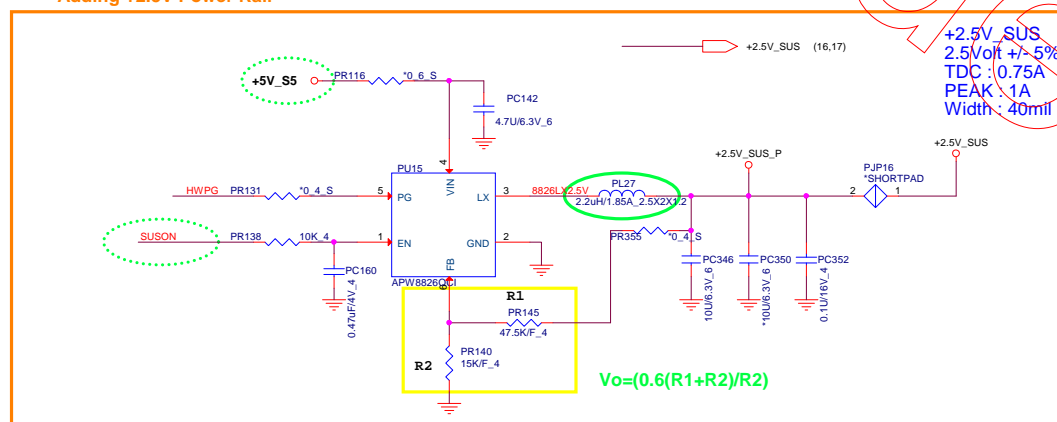
MOSFET	Package	ID (Ta=25°C)	Rds_on_max
TPCC8067-H	DFN3x3	9A	26m
TPCC8062-H	DFN3x3	27A	7.1m

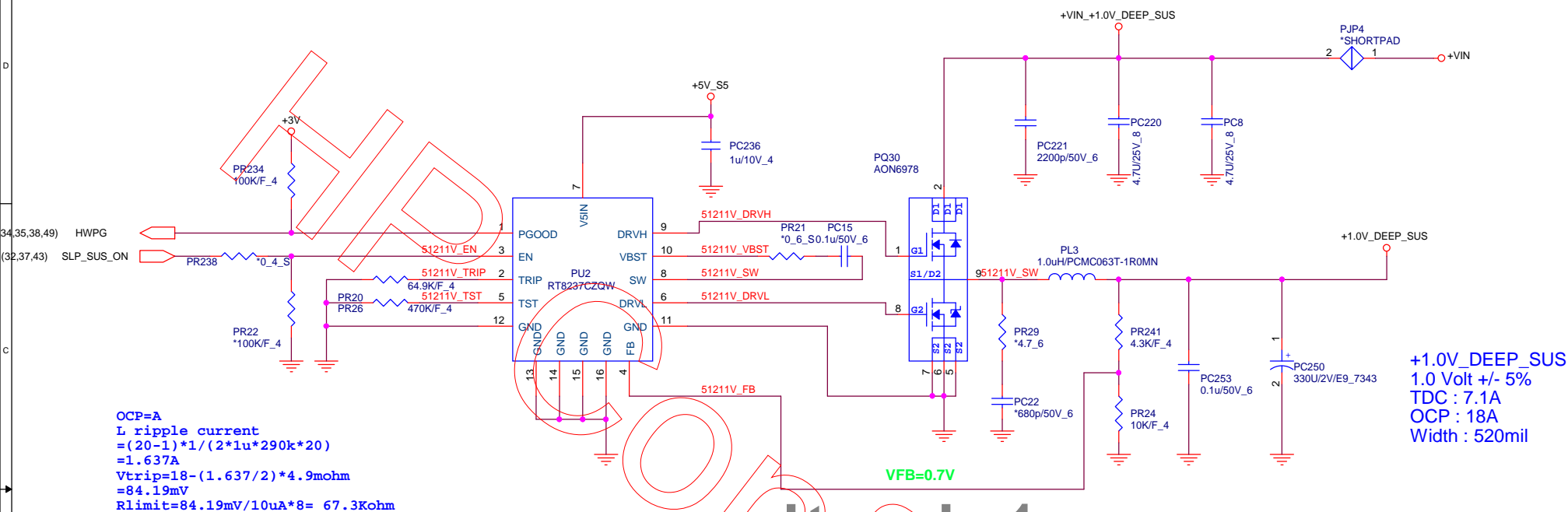
TDC : 0.45A
PEAK : 0.6A
Width : 40mil

+1.2VSUS
1.2 Volt +/- 5%
TDC : 8A
PEAK : 10A
OCP : 15A
Width : 280mil

$$V_o = (0.675 * (1 + (R1/R2)))$$

7/09 Chaneg DDR3L to DDR4
Adding +2.5V Power Rail





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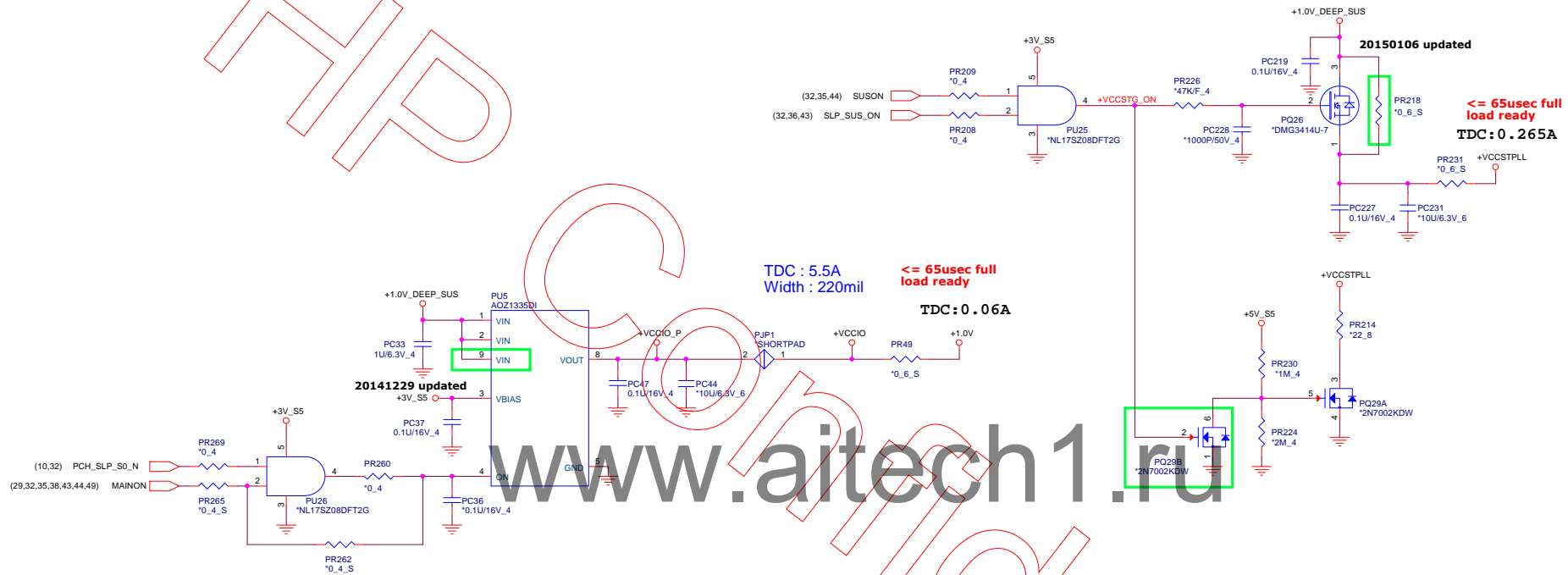
Quanta Computer Inc.

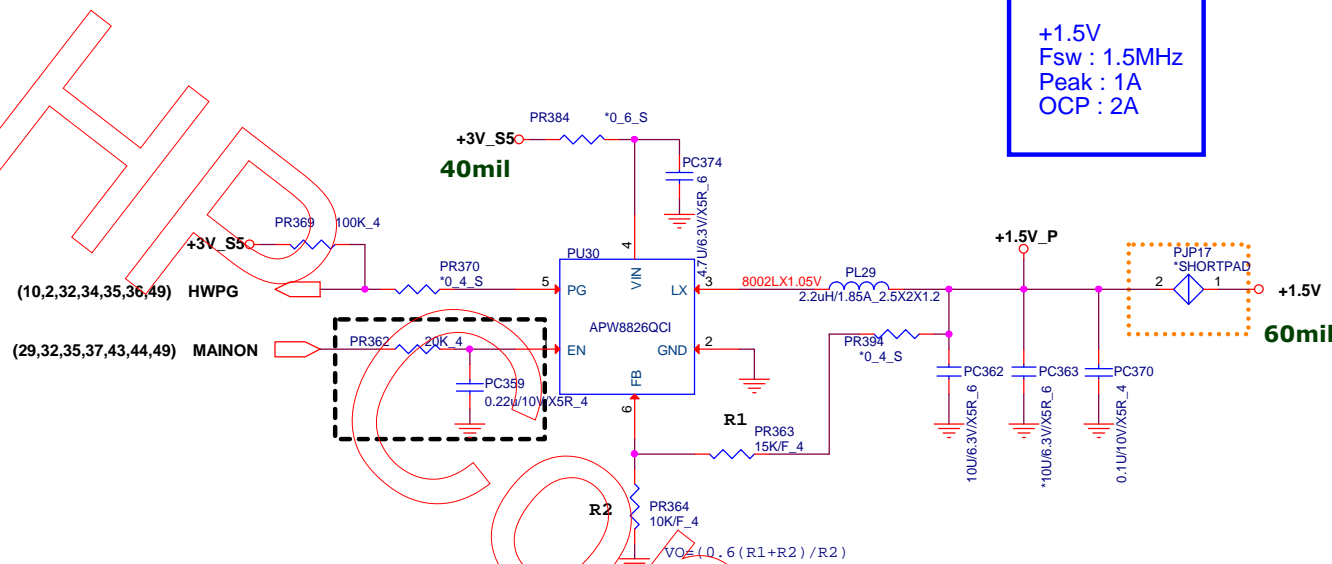
PROJECT : NL8E

Size	Document Number	Rev
	+1V_S5 (RT8237CZQW)	1A

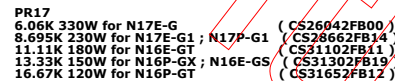
Date: Thursday, October 27, 2016 Sheet 36 of 66

+1.0V (10,2,32,6)
 +3V_S5 (10,12,14,21,23,25,26,27,28,31,32,34,38,39,43,49,52)
 +5V_S5 (10,26,28,29,34,35,36,39,40,41,42,43,44,45,46,47,49,50,51,52)
 +VCCIO (3,6)
 +VCCSTPLL (11,2,6)
 +1.0V_DEEP_SUS (10,11,14,36,39,44)

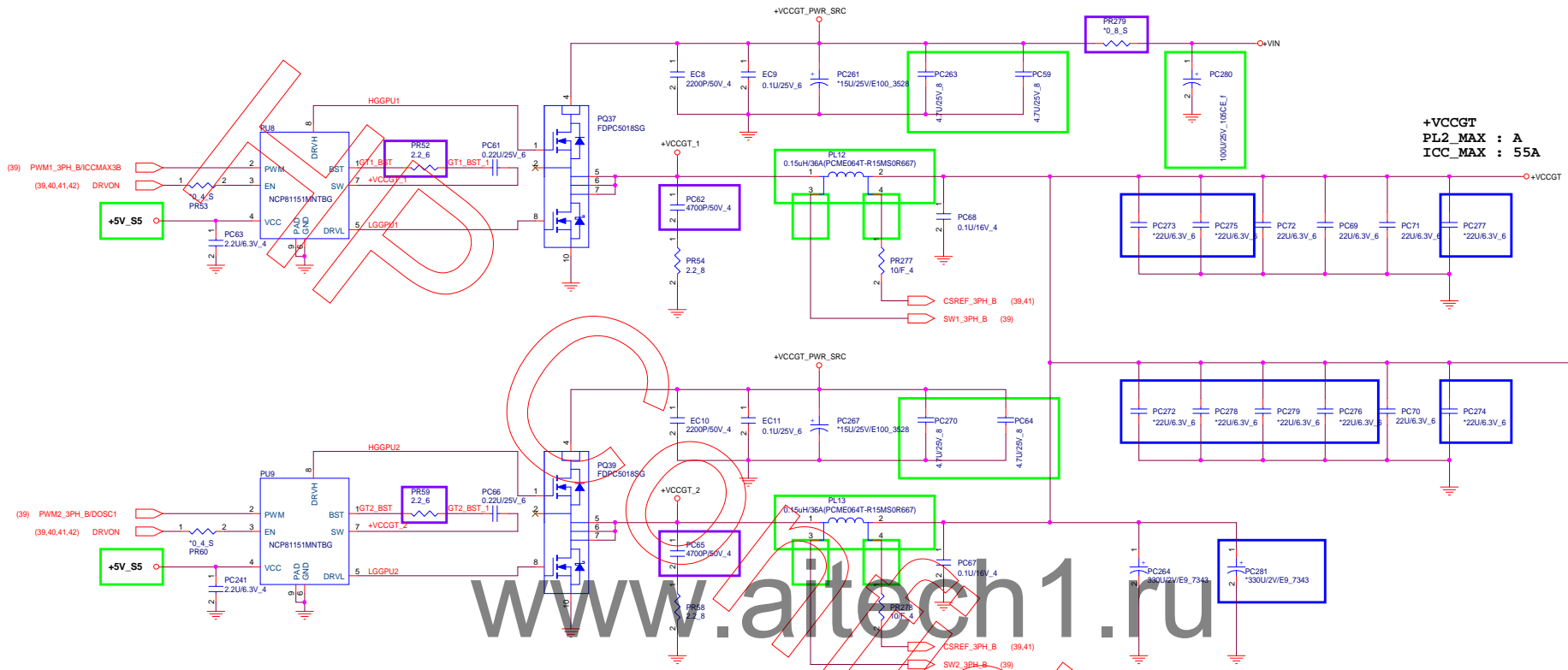




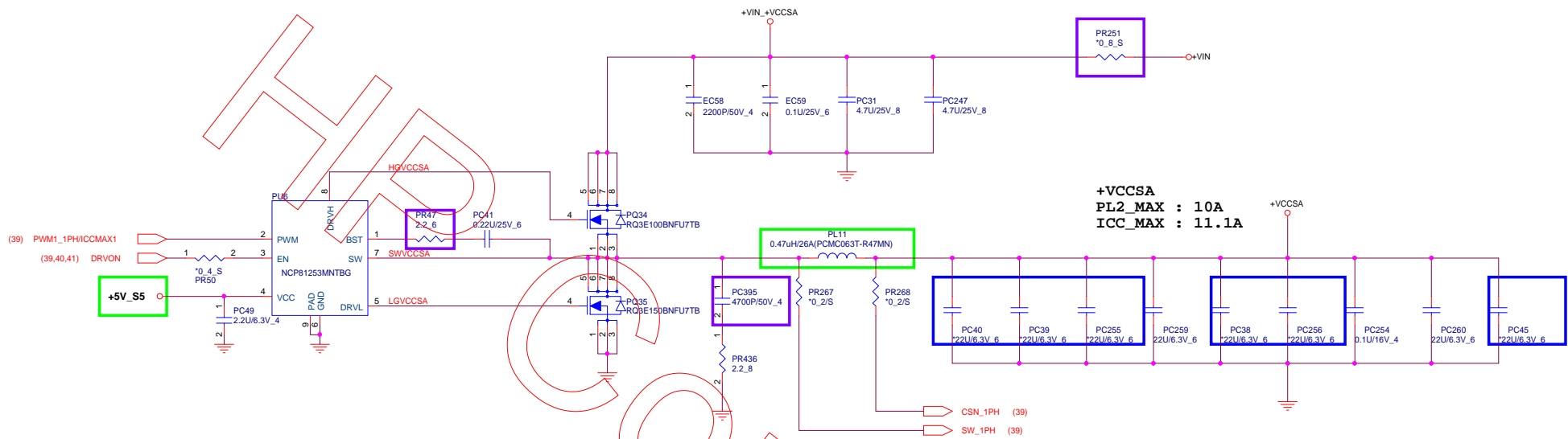
www.aitech1.ru





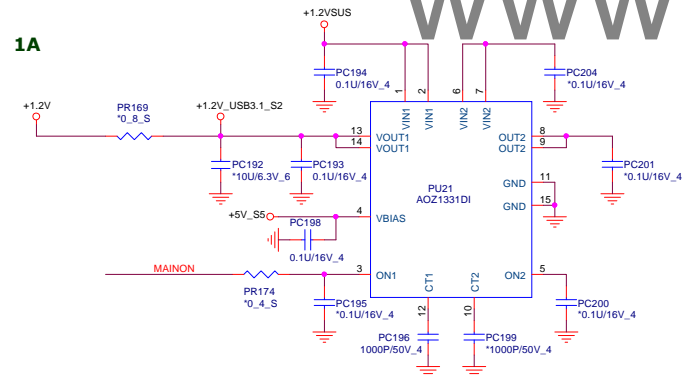
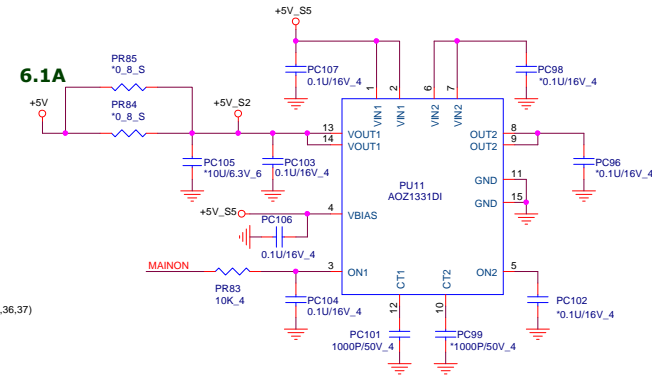
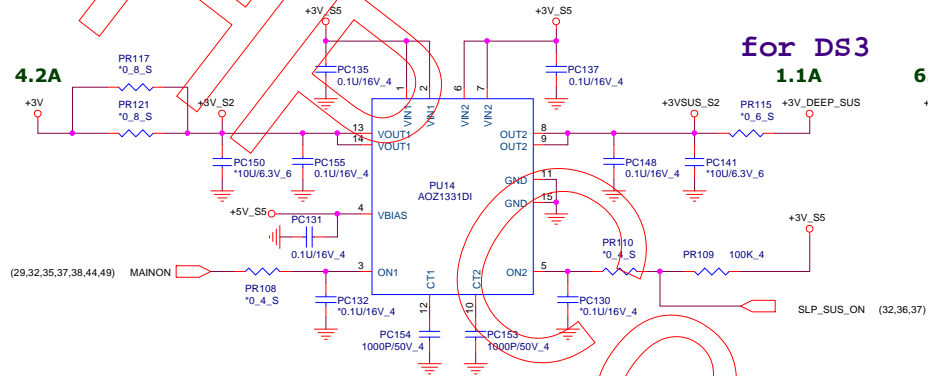


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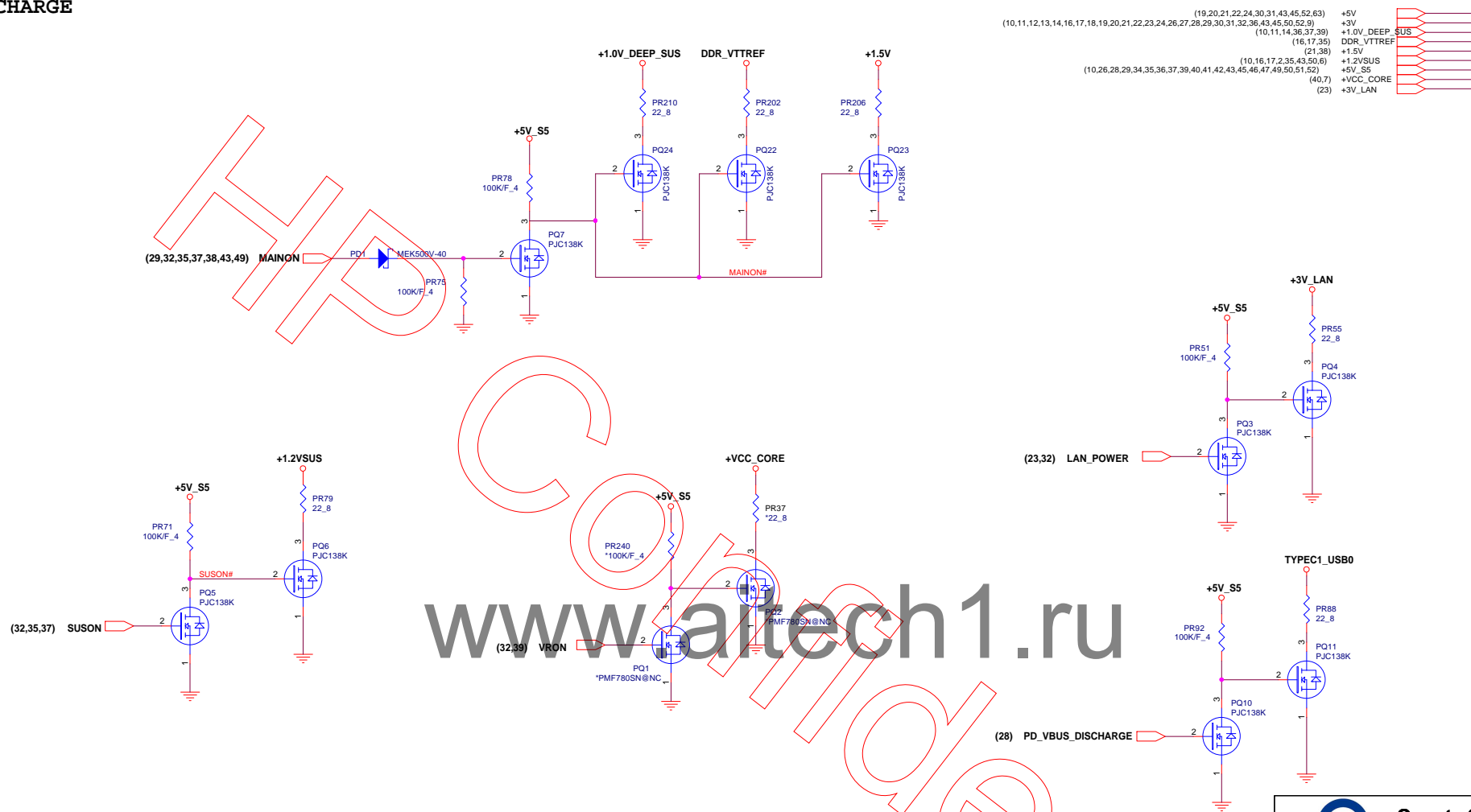
www.aitech1.ru

+3V (10,11,12,13,14,16,17,18,19,20,21,22,23,24,26,27,28,29,30,31,32,36,45,50,52,9)
 +6V (19,20,21,22,24,30,31,45,52,63)
 +3V_S5 (10,12,14,21,23,25,26,27,28,31,32,34,37,38,39,49,52)
 +5V_S5 (10,26,28,29,34,35,36,37,39,40,41,42,44,45,46,47,49,50,51,52)
 +VIN (18,33,34,35,36,39,40,41,42,47,50,52,63)




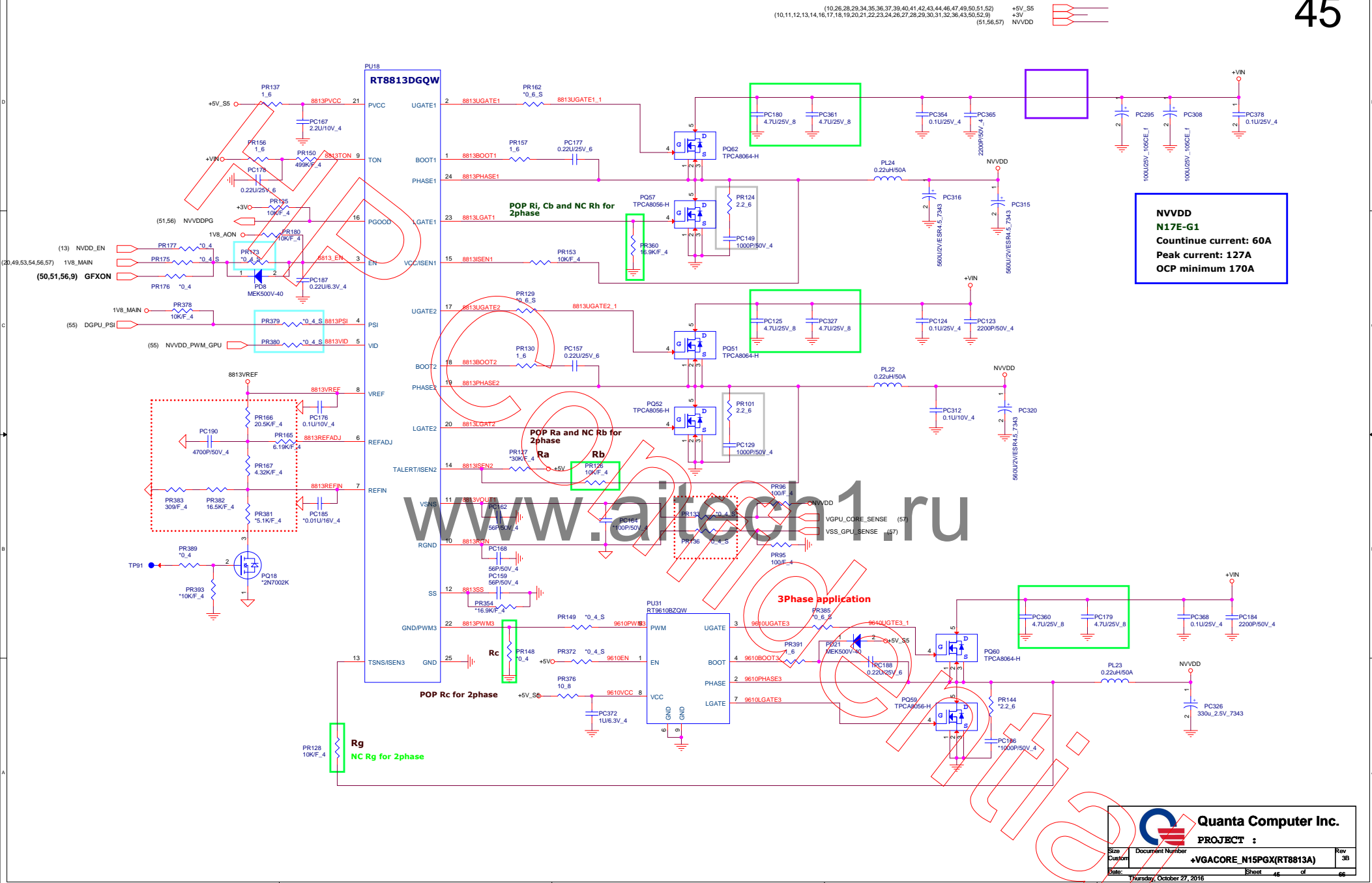
www.aitech1.ru

DISCHARGE

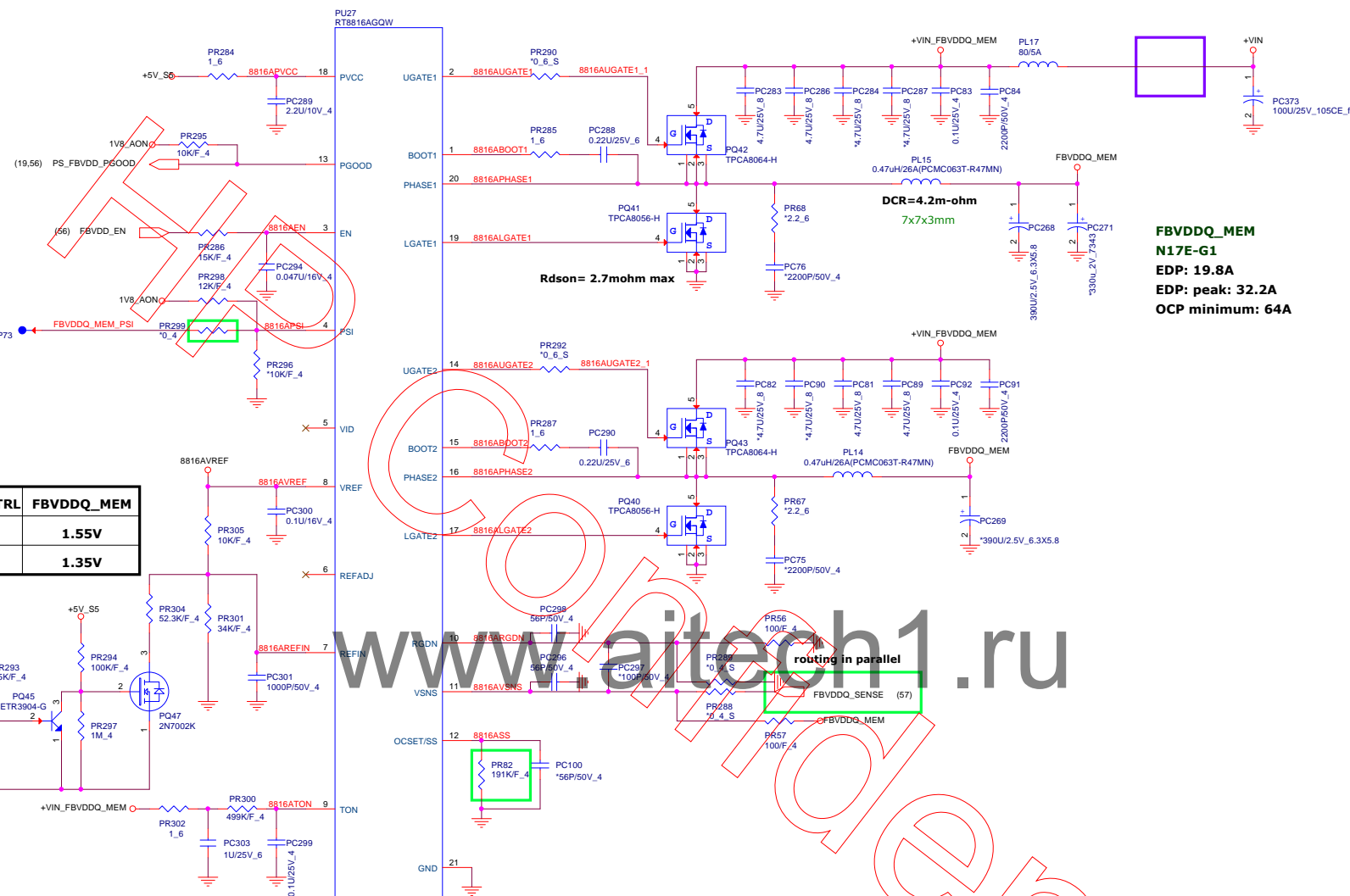


47

 Quanta Computer Inc.		
PROJECT :		
Size Custom	Document Number Discharge	Rev 3B
Date: Thursday, October 27, 2016	Sheet 44	of 66



9xxx




MEM_VDD_CTRL	FBVDDQ_MEM
1	1.55V
0	1.35V

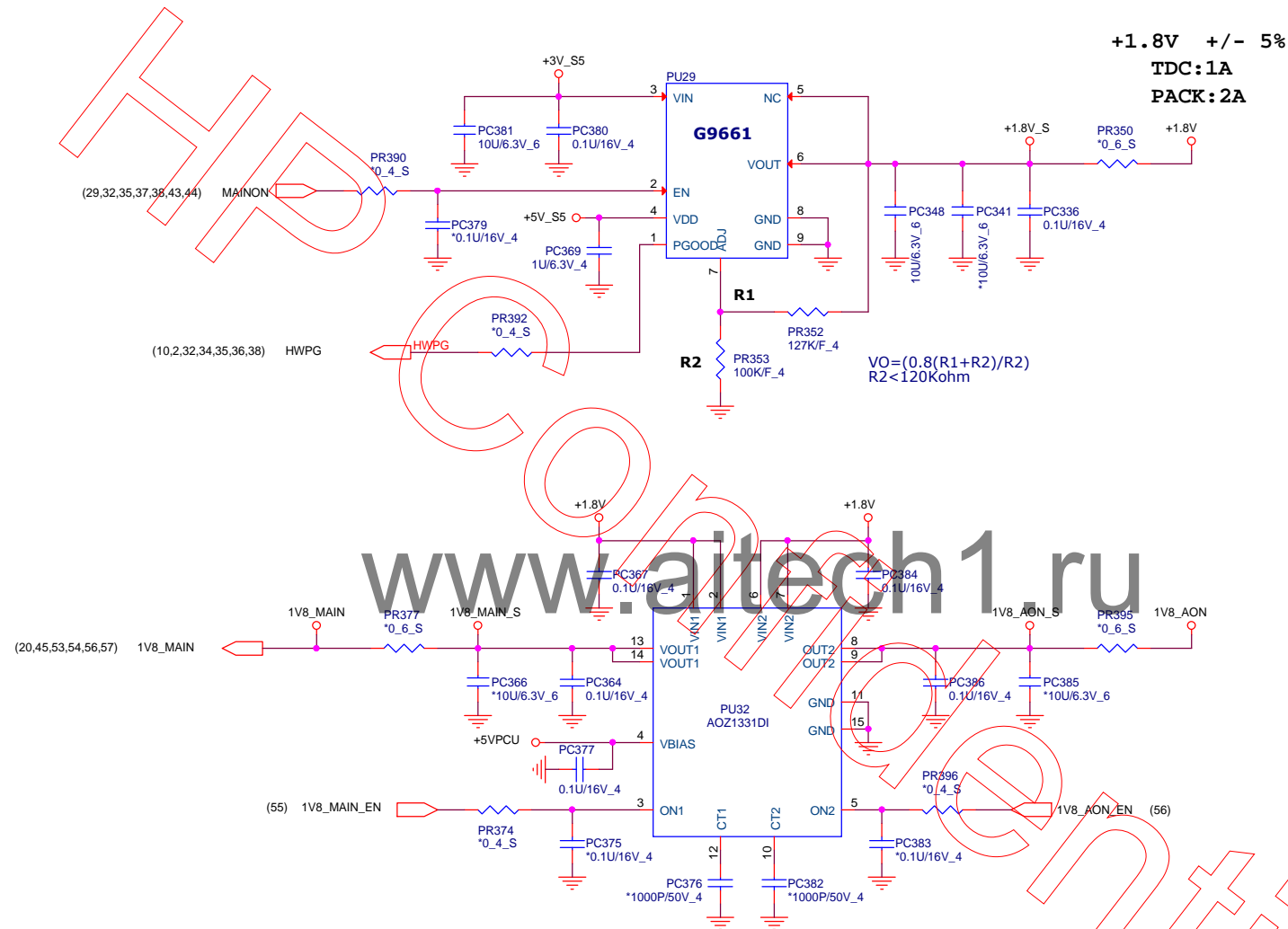
FBVDDQ_MEM
N17E-G1
EDP: 19.8A
EDP: peak: 32.2A
OCP minimum: 64A

routing in parallel

+VIN (18,33,34,35,36,39,40,41,42,50,52,63)
+5V_S5 (10,26,28,29,34,35,36,37,39,40,41,42,43,44,45,46,49,50,51,52)
FBVDDQ MEM (51,54,56,57,58,59)

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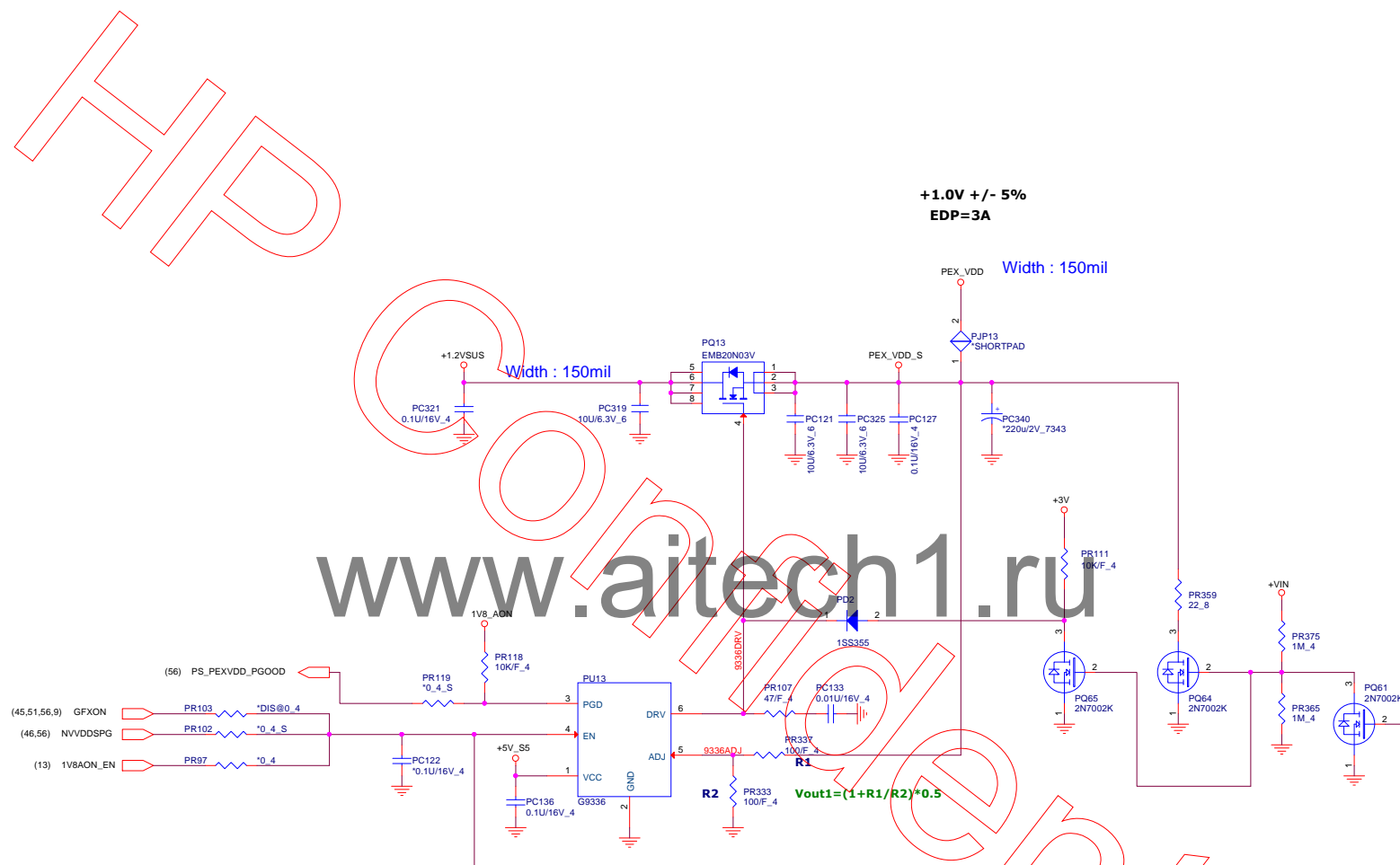
		Quanta Computer Inc.	
PROJECT :			
Size Custom	Document Number +1.35V_GPU(TP551211DSCR)	Rev 3B	
Date: Thursday, October 27, 2016	Sheet 48	of 66	

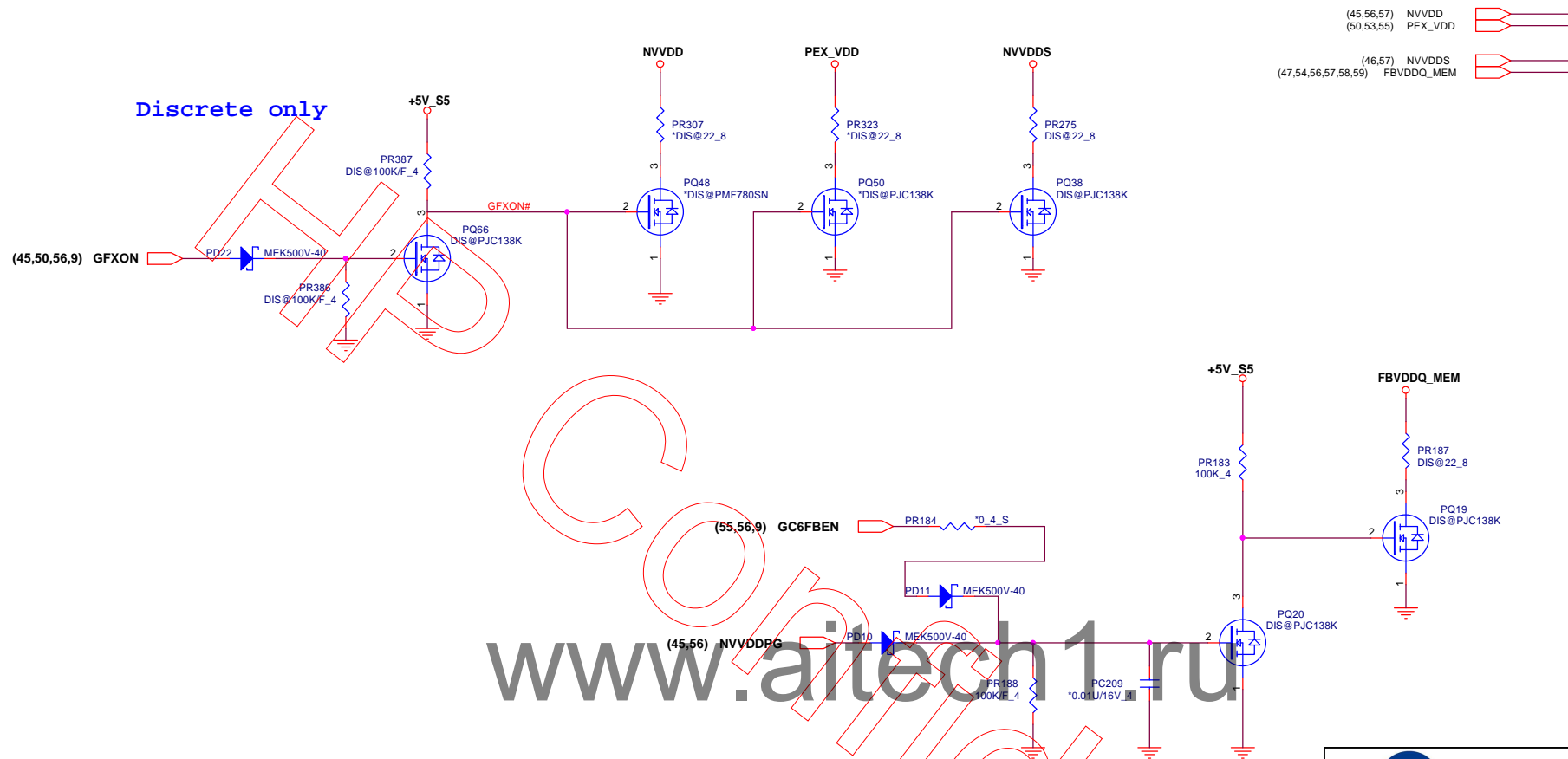



Quanta Computer Inc.

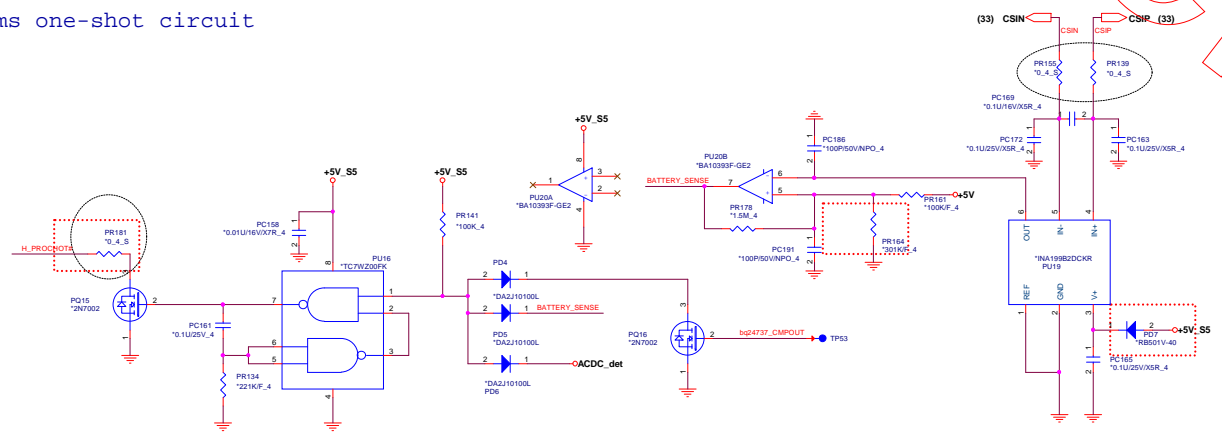
PROJECT :

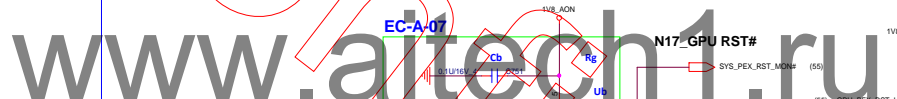
Size Custom	Document Number +1.8V (APW8713)	Rev 38
Date: Thursday, October 27, 2016	Sheet 49	of 66

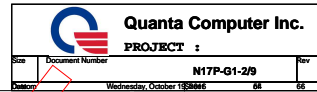


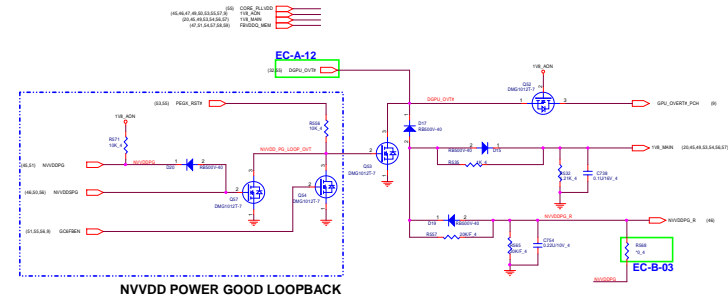
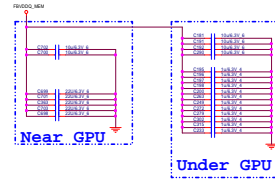
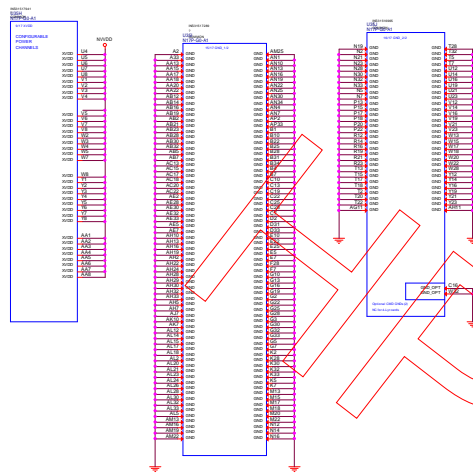


 Quanta Computer Inc.		
PROJECT :		
Size Custom	Document Number Discrete Discharge	Rev 3B
Date:	Thursday, October 27, 2016	Sheet 51 of 66



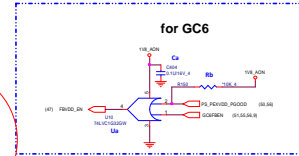




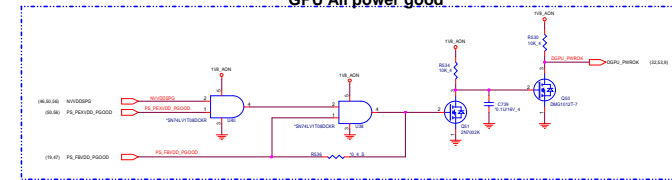


NVDD POWER GOOD LOOPBACK

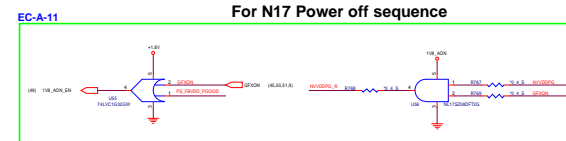
Overt temp ckt for NVDD and NVVDS



for GC6

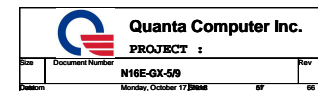


GPU All power good



For N17 Power off sequence

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CHANNEL A: 1024MB GDDR5x32

(47.51,54.56,57.58) FBVDDQ_MEM

Channel A
<0-31>

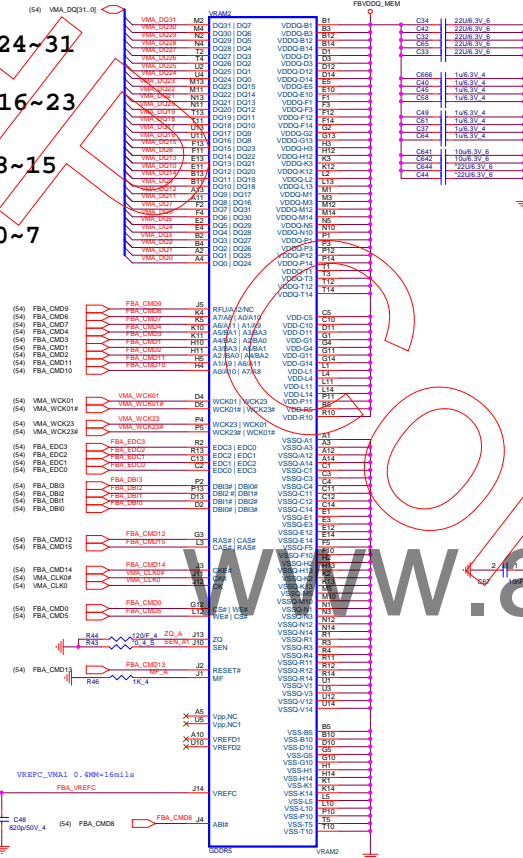
MF=0 Non-mirrored

QD24~31

QD16~23

QD8~15

QD0~7

Channel A
<32-63>

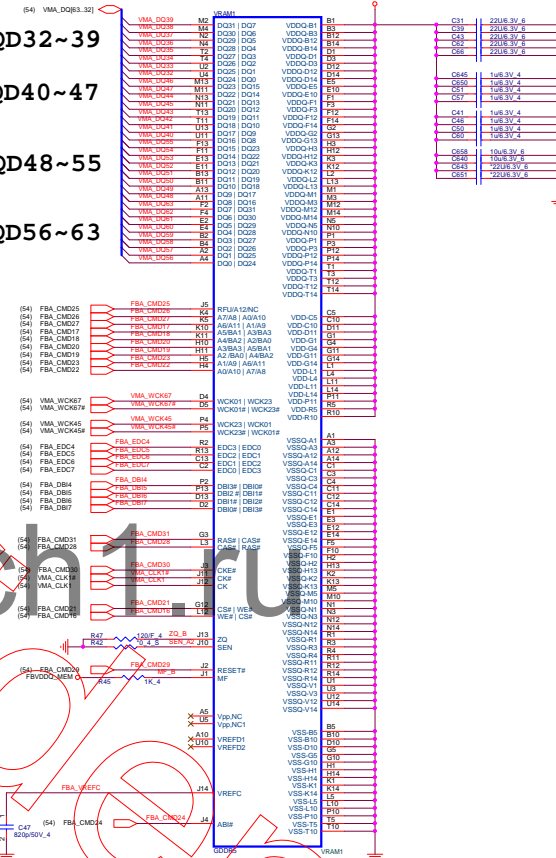
MF=1 mirrored

QD32~39

QD40~47

QD48~55

QD56~63

PROJECT : G38A
Quanta Computer Inc.

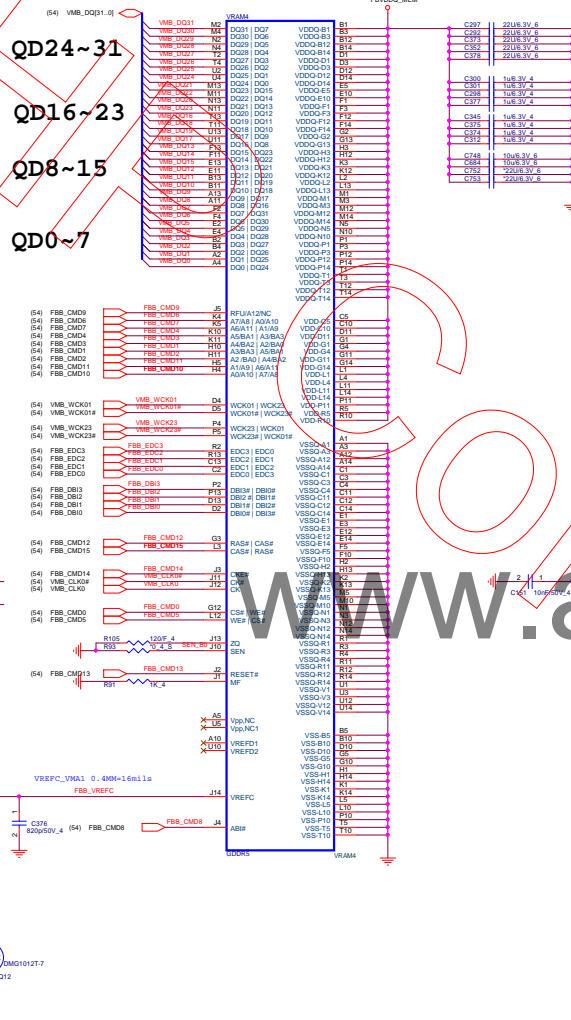
Doc No	Document Number	Rev
NB5	N17E-GX-6/8(GDDR5)	1A
Date	Wednesday, October 18, 2017 (Sheet 58 of 58)	

CHANNEL B: 1024MB GDDR5x32

(47.51,54,56,57,58) FBVDDQ_MEM

Channel B
<0~31>

MF=0 Non-mirrored

Channel B
<32~63>

MF=1 mirrored

PROJECT : G38A
Quanta Computer Inc.

Doc	Document Number	Rev
NB5	N17E-QX-7(GDDR5)	1A
Date	Wednesday, October 18, 2017	Sheet 59 of 66

HP
Confidential
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NB5

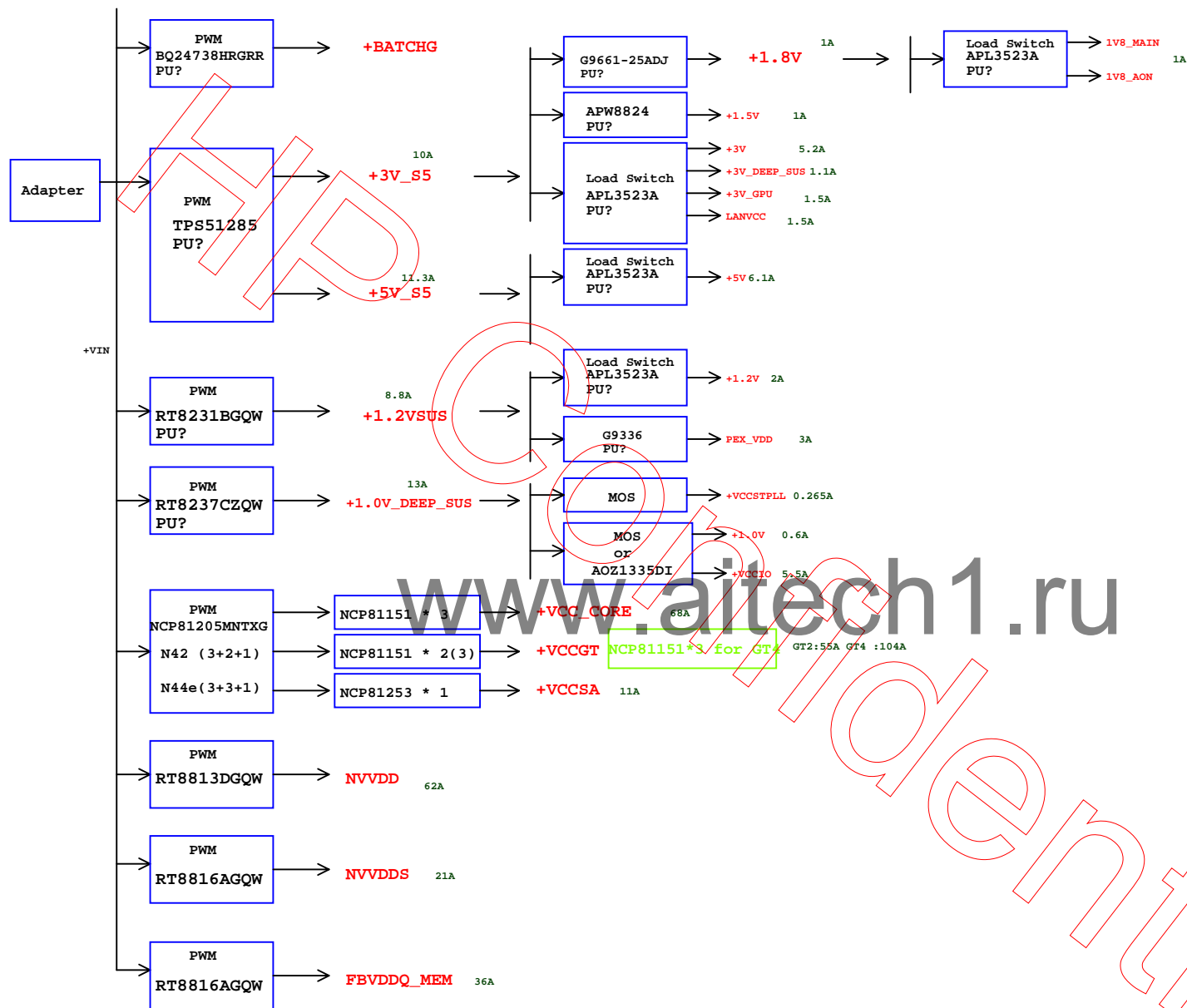
PROJECT : G38A
Quanta Computer Inc.

Size	Document Number	Rev
	N17E-GX-8/8(GDDR5)	1A
Date	Monday, October 17, 2016 13:00	86 of 86

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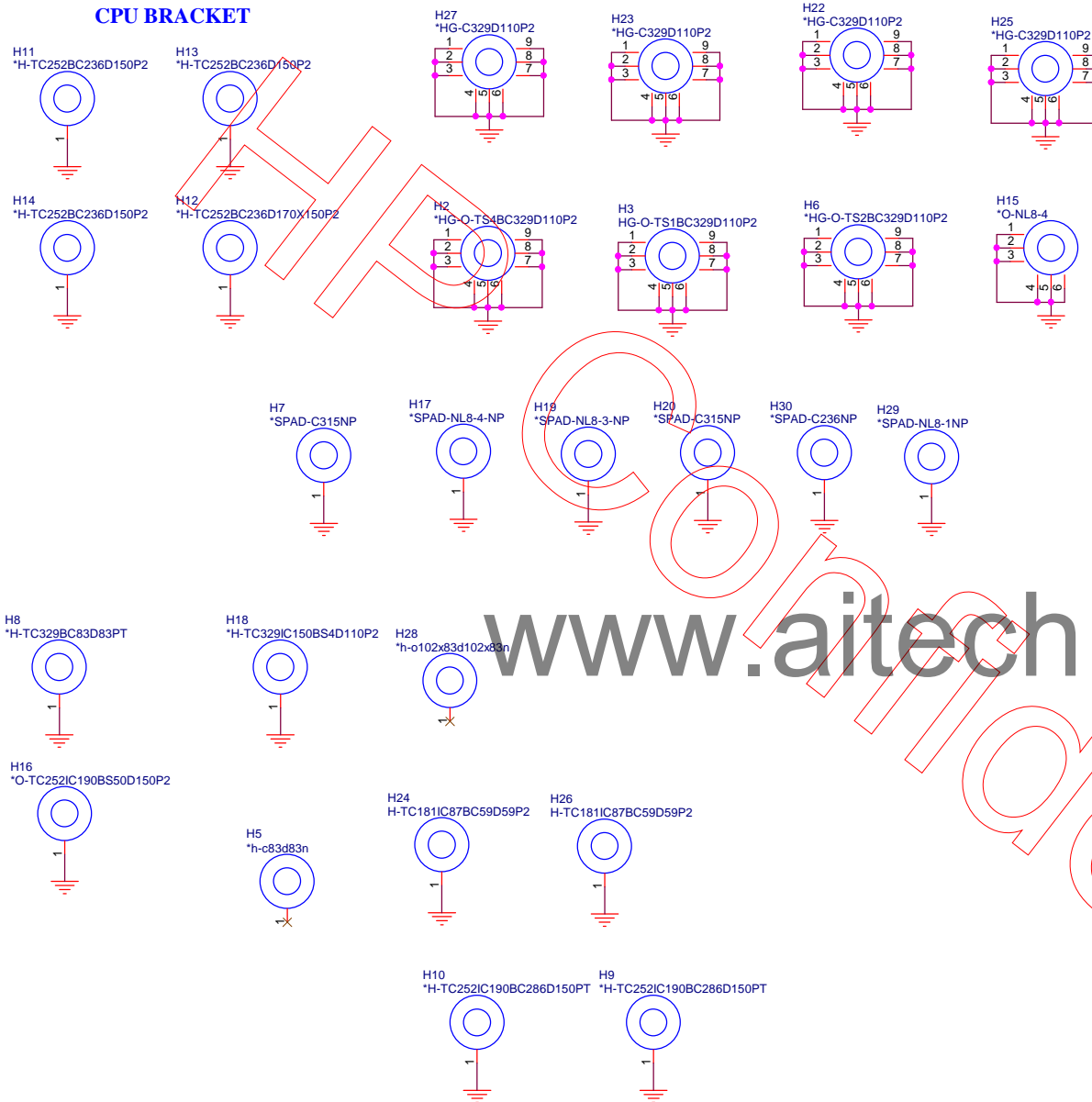
		Quanta Computer Inc.	
PROJECT :			
Size Custom	Document Number	blank	Rev 3B
Date:	Monday, October 17, 2016	Sheet 61 of 66	

Power Delivery Map

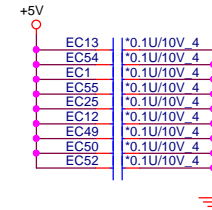




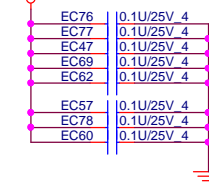
CPU BRACKET



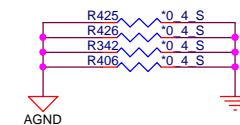
EMI



+VIN



ESD



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Quanta Computer Inc.		
PROJECT :		
Size	Document Number	Rev
Custom	HOLE	3B
Date:	Monday, October 17, 2016	Sheet 63 of 66




2016

SDV

SIV

EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
EC-A-01	19	8/10	R760	DP_Power add 0 ohm
EC-A-02	19	8/10	Q70,R761,R762	DP_HPDP change to dual mos type
EC-A-03	20	8/10	R763	HDMI_Power add 0 ohm
EC-A-04	12	8/10	Add U52,del U53	BIOS change socket to rom for B test
EC-A-05	26	8/10	C835	change 0402 correct PN
EC-A-06	26	8/10	C509,Y2	change cap,crystal for vendor recommend
EC-A-07	53	8/10	U39	change PN for 2nd source team recommend
EC-A-08	18	8/10	CN6	change to Vertical type &FP and upsidedown pin order
EC-A-09	27	8/10	CN1	change to type-C FP
EC-A-10	9	8/10	Q71,Q72,R766,C934	change GC6EN circuit
EC-A-11	56	8/10	U55,U56,R767,R768,R769	GPU power down sequence
EC-A-12	56	8/11		change from OVERT# to DGPU_OVT#
EC-A-13	55	8/17		Reserve GPU external bios for debug use
EC-A-14	30	8/19	R778,R779,R458,R448,R776,R777	cypress review CCG2 to Mux can't have cap
EC-A-15	10	8/19	R246	EC S5 leakage form AC PRESENT
EC-A-16	2,10	8/19	R780,R781,R782,R783	xHCI Debug Capability Compliance issue
EC-A-17	28	9/6	R161,R620	change Ilim to 93.1k ohm for 3A,asm R161 for type c hpd open drain
EC-B-01	13,19	10/17	R784,C785,C803	for DP to hdmi dongle cable issue
EC-B-02	20	10/17	C10,C621	change 0805 size to 0402 size
EC-B-03	56	10/17	R568	for remove R568 NV PWRGD path
EC-B-04	27	10/19	C816,C936	for FAE suggest
EC-B-05	10	10/26	R246	For ME check fail issue

		Quanta Computer Inc.	
PROJECT :			
Size	Document Number	Rev	
Custom	EC-list-1		
Date	Wednesday, October 26, 2016	Sheet	66 of 66